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VLSI Architecture of Encoding using Sols Technique for Reducing Power in DSRC

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ABSTRACT

Now a days DSRC plays a vital role. It is one way or two way short range to medium range communication. Such as safety applications, commercial vehicle applications, emergency warning systems for vehicle. DSRC adopts codes such as FMO/Manchester code. The codes are used to achieve dc-balance and signal reliability. This codes seriously limits the potential. The similarity oriented logic simplification technique (sols) is used here to overcome the limitation and also used to improve the hardware utilization rate. By using this two code power, delay, and area can be reduced. The proposed architecture will have less delay, area as compared to existing architecture. In this paper the architecture analyzed to reduce the number of components. Using both encodings the area, delay, and power is reduced in DSRC.

Keywords: DSRC (Dedicated Short Range Communication), FMO, Manchester encoder

INTRODUCTION

The DSRC is a protocol simplex or duplex range communication in the modern automotive industry. The DSRC mainly used for intelligent transportation systems. It can be briefly classified as vehicle to vehicle and vehicle to road-side communications. The DSRC can provide an inter communication between automobiles and road-sides for safety issues and public information announcement. These safety message include blind-spot, collision-alarm, inter cars distance etc. The vehicle to roadside communication mainly focuses on intelligent transport system such as electronic toll collection (ETC) system.

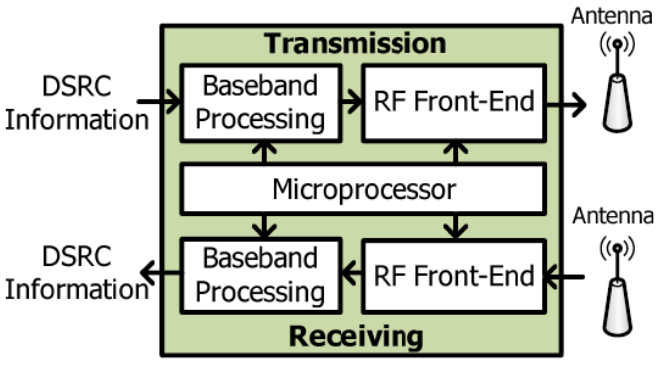

Fig1. *System architecture of DSRC*

The transceiver Architecture consists of two parts for transmission and receiving. The DSRC transceiver is classified as three basic modules (i) Microprocessor (ii) Baseband Processing (iii) RF-Front End. The Microprocessor used to interprets instructions from Media Access Control (MAC) to schedule the tasks of Baseband Processing and RF-Front End

The modulation, error correction, clock synchronization, encoding all is done by Base Band Processing. The RF Front End transmits the wireless signal through Antenna and receives the wireless signal through Antenna (i.e. physical transmission).All three modules co -operate with each to perform DSRC protocols. Several countries have been established DSRC Standards by various organizations With carrier frequency of 5.8GHz and 5.9 GHz, the data rate of individual organizations

as 500 Kbps, 27 mbps, 4 mbps. The Amplitude Shift Keying (ASK), Phase Shift Keying (PSK), Orthogonal Frequency Division Multiplexing (OFDM) are incorporates in modulation schemes. The encoding for downlink incorporates FMO (Flexible Macro-block Ordering and Manchester. The reliability of data signal is too important in DSRC standards compared to the data rate.

In common, the robustness issue, the transmitted signal waveform is expected to have zero mean and this is also referred as DC-balance. But due to the arbitrary binary sequence of transmitted signal. It is difficult to achieve DC balance. The purpose of FMO, Manchester codes can provide the transmitted signal with better DC-balance. The DC-balance is an important role in DSRC.

LITERATURE REVIEW

The literature [1] shows the Architectural view of Manchester encoder for optical communication, Here the Manchester encoder is designed by using CMOS inverter and the gate inverter as the switch. The operation frequency is 1 GHz and implemented by 0.35 µm CMOS technology. The Literature [2] shows that the design of Manchester encoder by NMOS device instead of switch [1] with 90 nm CMOS technology. The maximum operation frequency is as high as 5 GHz. The literature [3] explains high-speed VLSI Architecture of Manchester and miller encodings for RFID application with 0.35 µm CMOS technology and maximum operation frequency is 200 MHz The literature [4] also proposes the Architecture of Manchester encoding for Ultra High Frequency (UHF) RFID tag emulator. By using FSM, the hardware Architecture is constructed and implemented in FPGA prototyping system, the maximum operational frequency is 256 MHz

PRINCIPLES OF FMO CODE AND MANCHESTER CODE

FMO Encoding

The FMO having the following three rules.

(1) If X is the logic-0, The FMO code has the transition between the A and B.

(2) If X is the logic-1, There is no transition is allowed between the A and B.

(3) The transition is allocated in each FMO code.

The wave form is given below the following diagram. The FMO having the clock and then the x.the clock and then the cycle having the cycle in each transaction.

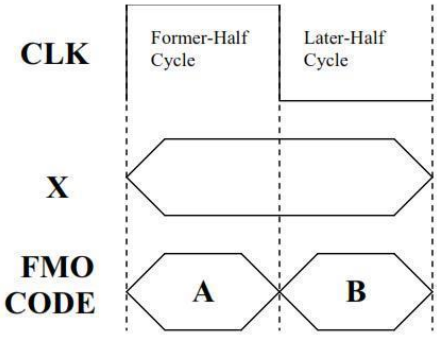

Fig2. *Coding of FMO*

Manchester Encoding

The Manchester encoding is realized with the XOR operation for using the CLOCK and X. The clock always has a transition within the one cycle.

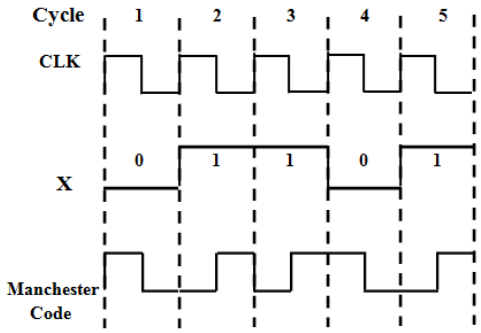

Fig3. *Manchester Encoding*

THE STATE CODE PRINCIPLE FOR FMO/MANCHESTER

The Manchester encoding is an XOR operation only. The FMO code starts with the FSM principle. The FSM of FMO code classified into four states. The four states as shown in the below figure.

Suppose the initial state is S1, and its state code is 11 for A and B, respectively.

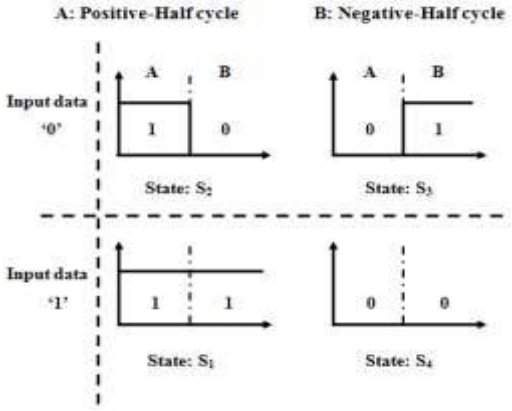

Fig4. *FSM of FMO*

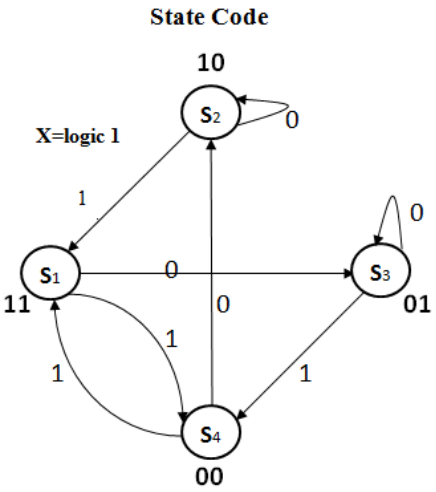

Fig5. *State diagram of FMO*

1) If the X is logic-0, the state-transition must follow both rules for FMO1 and 3. The only one next-state that can satisfy both rules for the X of logic-0 is S3. If the X is logic-1, the state-transition must follow both rules for FMO 2 and 3. The only one next-state that can satisfy both rules for the X of logic-1 is S4. Thus, the state-transition of each state can be completely constructed. The FSM of FMO can also conduct the transition table of each state A(t) and B(t) represent the discrete-time state code of current-state at time instant t. Their previous-states are denoted as the A(t − 1)and the B(t − 1), respectively. With this transition table, the Boolean functions of A(t) and B(t) are given as

2) $$A(t) = B(t-1)$$

$$B(t) = X \oplus B(t-1)$$

With both A(t) and B(t), the Boolean function of FMO code is denoted as

$$CLK\ A(t) +\sim CLK\ B(t)$$

Table1. *State Transition Table*

Previous state		Current state			
A(t-1)	B(t-1)	A(t)		B(t)	
		X=0	X=1	X=0	X=1
1	1	0	0	1	0
1	0	1	1	0	1
0	1	1	0	1	1
0	0	1	1	0	1

HARDWARE ARCHITECTURE OF FMO/MANCHESTER CODE

The hardware Architecture is mainly used to analyze the hardware utilization of both FMO, Manchester encoder. The hardware Architecture of Manchester encoding is simple XOR operation. But it is very difficult to construct hardware Architecture of FMO compare with Manchester. To construct the FMO hardware Architecture should start with FSM of FMO.

Table2. *HUR of FMO and Manchester encodings*

coding	Active components/ total components	HUR
FMO	6(86)/7(98)	85.71%
MANCHESTER	2(26)/7(98)	28.57%
AVERAGE	4(56)/7(98)	57.14%

The hardware architecture of the FMO/Manchester code is shown below. The top part is denoted the FMO code and then the bottom part is denoted as the Manchester code in FMO code the DFFA and DFFB are used to store the state code of the FMO code and also mux_1 and not gate is used in the FMO code. When the mode=0 is for the FMO code the Manchester code is developed only using the XOR gate and when the mode=1 is for the Manchester code the hardware utilization rate is defined as the following.

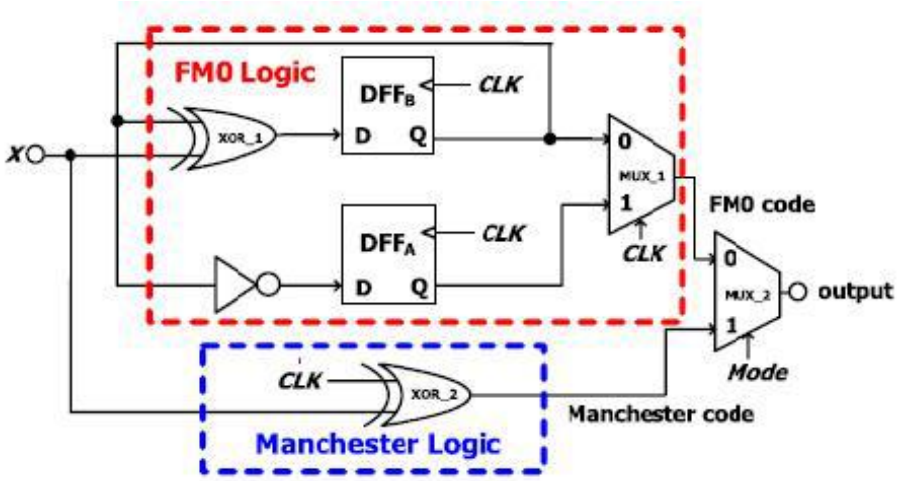

Fig6. *VLSI HUR of FMO and Manchester encoder*

*HUR = (Active components/ Total components)*100*

The active components means the components are work in the both FMO and Manchester code. The total components means the number of the components are present in the hole circuit. For both the encoding methods the total components is 7.for the FMO code the total component is 7 and then the active component is 6.in Manchester code the total component is 7 the active component is 2.in both coding having 98 transistors are used without SOLS. The FMO having 86 transistor, and then the Manchester having the 26 transistor the average for both coding is 56 transistors .In proposed work reduce the total components from 7 to 6 and reduce the transistor counts. In this paper two multiplexer is used in proposed work reduce two multiplexer from one multiplexer, when reduce the multiplexer the total components are reduced the area and then the power consumption also reduced.

FMO AND MANCHESTER ENCODER USING SOLS TECHNIQUE

The SOLS technique is classified into two parts area compact retiming and balance logic operation sharing

Area Compact Retiming

For FMO the state code of the each state is stored into DFFA and DFFB .the transition of the state code is only depends on the previous state of B(t-1) instead of the both A(t-1) and B(t-1). The previous state is denoted as the A(t-1) and then the B(t-1) and then the current state is denoted as the A(t) and then the B(t) Thus, the FMO encoding just requires a single 1-bitflip-flop to store the previous value B(t−1).If the DFFA is directly removed, a non synchronization between A(t) and B(t)causes the logic fault of FMO code.

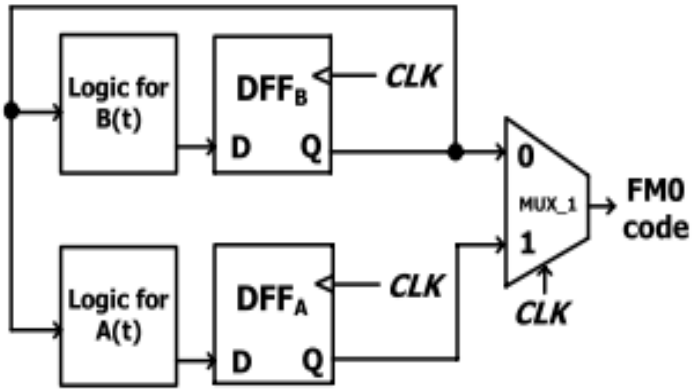

Fig7. *Area compact retiming*

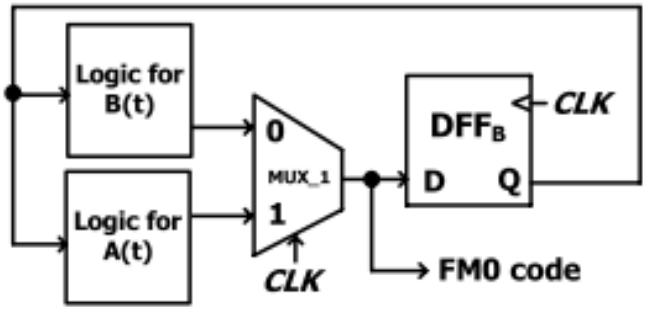

Fig8. *FMO of without area compact retiming*

To avoid this logic-fault, the DFFB is relocated right after the MUX−1, where the DFFB is assumed be positive-edge triggered flip flop. At each cycle, the FMO code, comprising A and B, is derived from the logic of A(t) and the logic of B(t), respectively. The FMO code is alternatively switched between A(t) and B(t) through the MUX−1 by the control signal of the CLK. In the Q of DFFB is directly updated from the logic of B(t)with 1-cycle latency. when the CLK is logic-0, the B(t) is passed through MUX−1 to the D of DFFB. Then, the upcoming positive-edge of CLK updates it to the Q of DFFB. The timing diagram for the Q of DFFB is consistent whether the DFFB is relocated or not. The transistor count of the FMO encoding architecture without area-compact retiming is 72,and that with area-compact retiming is 50. The area-compact retiming technique reduces 22 transistors.

Balance Logic Operation Sharing

The Manchester encoding is derived using the XOR operation. the equation of the XOR gate is given below.

X ⊕CLK=X CLK+~ X CLK

The concept of balance logic-operation sharing is to integrate the X into A(t) and X into B(t).the FMO and Manchester logics have a common point of the multiplexer like logic with the selection of the CLK. the diagram for the balance logic operation sharing given the following.

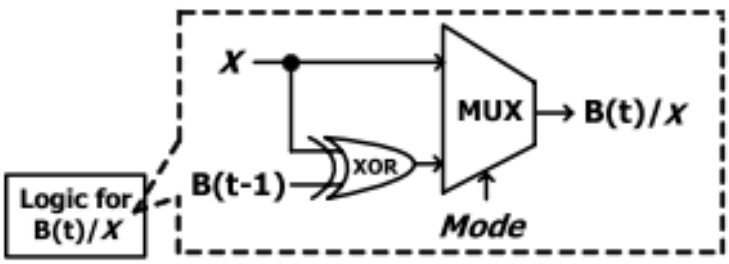

Fig9. *Balance logic operation sharing*

The A(t) can be derived from an inverter of B(t − 1), and X is obtained by an inverter of X. The logic for A(t)/X can share the same inverter, and then a multiplexer is placed before the inverter to switch he operands of B(t −1) and X. The Mode indicates either FMO or Manchester encoding is adopted.

The similar concept can be also applied to the logic for B(t)/X. Nevertheless, this architecture exhibits a drawback that the XOR is only dedicated for FMO encoding, and is not shared with Manchester encoding. Therefore, the HUR of this architecture is certainly limited. The X can be also interpreted as the $\boldsymbol{X} \oplus 0$, and thereby the XOR operation can be shared with Manchester and FMO encodings, where the multiplexer irresponsible to switch the operands of B(t−1) and logic-0. This architecture shares the XOR for both B(t) and X, and there by increases the HUR. When the FMO code is adopted, the CLR is disabled, and the B(t −1) can be derived from DFFB .

Hence, the multiplexer can be totally saved, and its function can be completely integrated into the relocated DFF. The logic for A(t)/X includes the MUX−2 and an inverter. Instead ,the logic for B(t)/X just incorporates a XOR gate. In the logic for A(t)/X, the computation time of MUX−2is almost identical to that of XOR in the logic for B(t)/X. However, the logic for A(t)/X further incorporates an inverter in the series of MUX−2. This unbalance computation time between A(t)/X and B(t)/X results in the glitch to MUX−1,possibly causing the logic fault on coding. To alleviate this unbalance computation time, the architecture of the balance computation time between A(t)/X and B(t)/X The XOR in the logic for B(t)/X is translated into the XNOR with an inverter, and then this inverter is shared with that of the logic for A(t)/X. This shared inverter is relocated backward to the output of MUX−1. Thus, the logic computation time between A(t)/X and B(t)/X is more balance to each other.

RESULT ANALYSIS

FM0 Encoding and Manchester Encoding are be simulated by using Xilinx software through Verilog HDL coding.

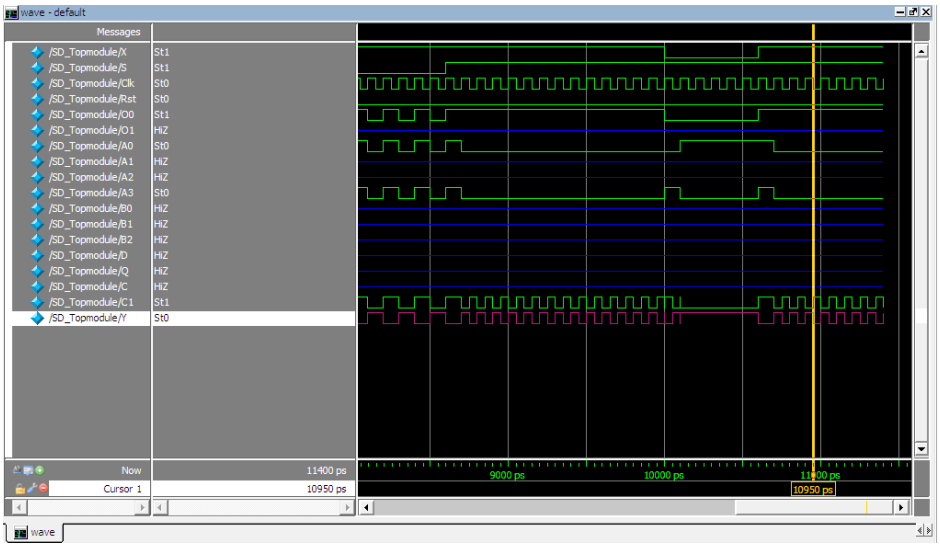

Fig10. Balanced FMO encoding

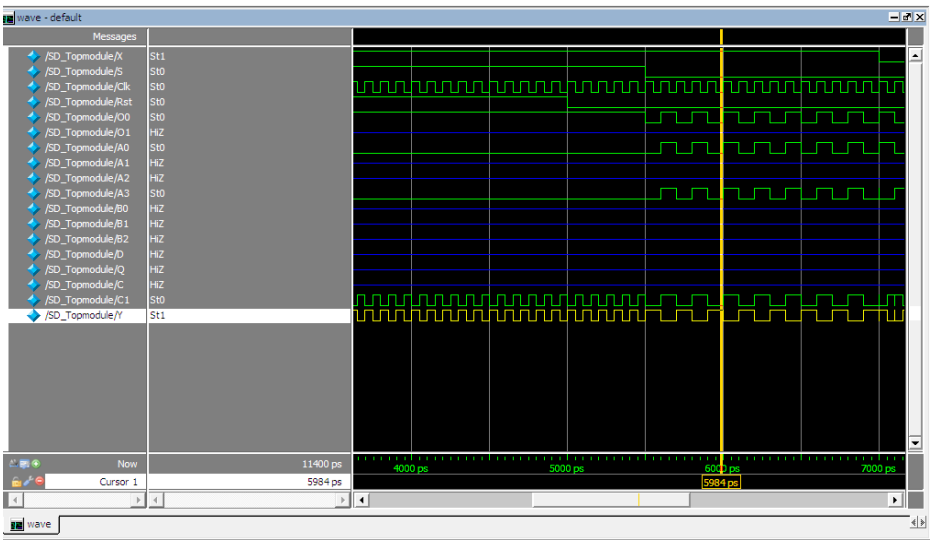

Fig11. *Balanced Manchester encoding*

Depending upon the data value output to be changed through selecting Reset, CLR and MODE The initial hardware architecture does not have CLR function and have only MODE function to select FM0 or Manchester operation

CONCLUSION

The hardware utilization is limited by the diversity between both FMO and Manchester encodings in VLSI Architectural design. This limitation is analyzed in detail. This paper shows the encoding technique of FMO and Manchester with SOLS technique eliminates the limitation of hardware utilization by two core techniques (a)Compact of Area Retiming (b)Sharing of Logic Operation. Using compact of area retiming, the number of transistor is reduce to 22 transistors. The sharing of logic operation combines FMO and Manchester encodings. The maximum operating frequency of Manchester, FMO encodings are 2 GHz, 900MHz with consumption of power 1.58mW, 1.14mW respectively. The encoding technique used in DSRC standards is fully supported in America, Europe and Japan.

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