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Design of Low Power and High Performance Radix-8 Multiplier

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Abstract: *A One-bit adder is designed using modified complementary pass transistor logic (MCPL). The proposed adder is implemented in 8×8 bit high radix multiplier to achieve high speed, low area and less power dissipation. This circuit is simulated by using DSCH2 (Micro Wind) schematic design tool. The 8×8 bit high radix multiplier is then compared with Baugh-Wooley multiplier, Brawn multiplier and high radix multiplier to show the better performance in terms of power, delay and power-delay product.*

Keywords: *Radix-8 Multiplier, Baugh-Wooley Multiplier, Brawn Multiplier.*

1. INTRODUCTION

There are infinite number of ways to perform multiplication but still many researchers working in this field, show the importance of multiplication. Many multiplier circuit designs have been proposed, which manage to operate at lower propagation delays with lesser power dissipation and a lower power rating of input bits [I].Multiplier is generally used in Digital Signal Processor (DSP) devices. In VLSI design, researchers mainly concentrate on area, speed and power dissipation. High speed multipliers include Braun multiplier, Booth multiplier, Parallel multiplier and high radix multiplier [2]. Basic multiplication can be realized by the shift add algorithm by generating partial products and adding successive properly shifted partial products. Thus multiplication is proportional to the number of partial products to be added [3]. In all multiplier circuits, two types of adder cells are present. They are half adder and full adder. For the adder to work in high speed, implementing the adder in any one of the high speed techniques is essential. Circuit delay depends on the number of inversion levels. Circuit size depends on the number of transistors in the circuit. Power dissipation depends on the switching activity [4]. Pass transistor can be synthesized by using two methods. One is using Binary Decision Diagrams and the other is a library based design [5]. Various type of full adder has been investigated in [6- 7].Various technique of multiplier has been investigated in [8-12].The design of radix-4 multiplier algorithm is taken from [13] and is applied for our Radix-8 multiplier but our design is different from that paper.

2. ANALYSIS OF ADDERS

One-bit adder is proposed by using the modified complementary pass transistor logic. Advantages of using this method are high speed, lower area, low propagation delay. This full adder is then implemented in high radix multiplier. It is then compared with the carry save array multiplier Brawn multiplier and Baugh-Wooley multiplier. Simulation results must be fully based on Complementary Metal Oxide Semiconductor (CMOS) design rule. One-bit full adder can be implemented by using the combination of both the multiplexing control input techniques and complementary pass transistor logic.

The proposed full adder is shown in the Figure 1.

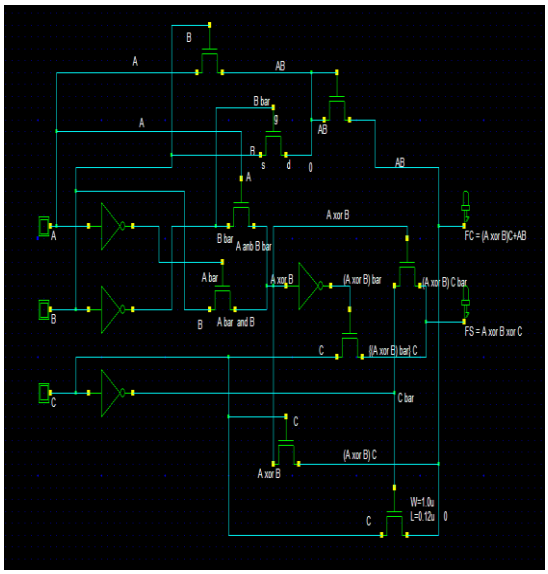

Figure I. *Proposed Full Adder*

Complementary Pass Transistor Logic (CPL)

Complementary Pass Transistor Logic (CPL) provides high-speed, full-swing operation and good driving capabilities due to the output static inverters and fast differential stage of cross-coupled PMOS transistors. But due to the presence, of a lot of internal nodes ad static inverters, there is a large power dissipation.

Multiplexing Control Input Techniques (MCIT)

The multiplexing control input technique is developed using the karnaugh map which is drawn from the truth table of full adder. According to sum and carry Boolean identities, we can generate the pass-transistor functions. When expression result=l pass transistor function is represented by the input variables and when expression result= 0 pass transistor function is represented by the complement of the input variables. To generate the Pass Transistor Function for 'n' input variable functions, we use 'n-1' as control input data. Simplified sum and carry expression are given as:

$$C=AB+AC+BC \quad (2.1)$$

$$S= A'B'C+ A'BC'+ AB'C'+ ABC \quad (2.2)$$

In CPL techniques, there are many drawbacks. To overcome this, we combine both the CPL techniques and MCIT techniques. Drawbacks occur in CPL due to the body effect, source follower action, and high power leakage. If the CPL is not cross coupled, then it results in low performance and limited fanout.

3. Analysis of Multipliers

A. Radix 8 Multiplier

The MULTIPLEXER is functioned such that the first two bits of the multiplexer, x, will be grabbed to determine the first partial product and shifted to the next 2 bits of the multiplier to determine the successive partial products by repeating the same process. For a 8 bit radix-8 multiplier, two partial products will be generated. As a result, half of the partial product will be reduced compared to other method. The radix-8 multiplier is shown in the figure 2. It consists of the following: Partial product selector, carry save adder (csa), half adder, and Full adder. In this multiplier, two bits per cycle are considered. Eight multiples are pre-computed; 1a is the multiplicand value, 2a is the shifted version of a. In half adder, CPL technique is applied, and in full adder, the proposed one is implemented. Partial Product Selector is formed by AND gates. All PPS, csa8 and csa10 are connected according to the design flow. In eight bit radix-8 multiplier, 2 partial products will be produced. Partial product is reduced to half as compared to the shift and add method.lt is then simulated and ten finally compared with other multipliers. Radix-8 multiplier is shown in figure 2.

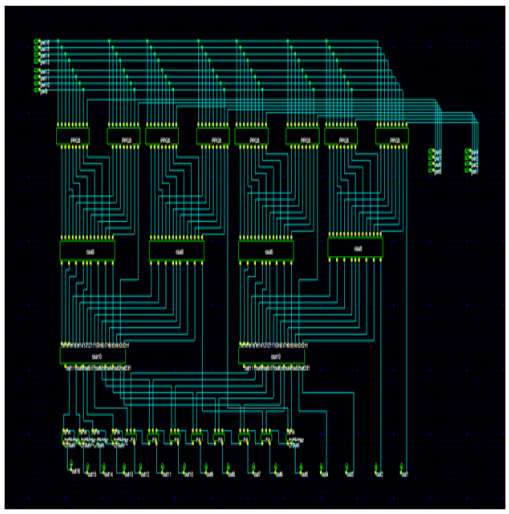

Figure 2. *Radix-8 multiplier*

For example consider 11001011x 10101010.

In this, 11001011 is the multiplicand value, a.

10101010 is the multiplier value, X.

2a value is the shift version of a

i.e.011001011.

The calculation is as follows.

00000000 - p(0)	00000000 - R(0)
0110010110 - 2ax1x0	0110010110 - 2ax5x4
0110010110 - p(0) + 2ax1x0	0110010110 - R(0) + 2ax5x4
0001100101 10 - p(1)	0001100101 10 - R(1)
0110010110 - 2ax3x2	0110010110 - 2ax7x6
01 1111101110 - p(1) + 2ax3x2	0111111101110 - R(1)+ 2ax7x6
00011111101110 - p(2)	
00000111111101110 - p(3)	

00000111111101110	- p(3)
011111101110	- R(1)+ 2ax7x6
1000011011001110	- Final Result

B. Carry Save Array Multiplier

The Carry Save Array (CSA) multiplier is a linear array multiplier. The linear multiplier propagates data down through the array cell. Each row of CSAs adds one additional partial-product to the partial sum. As the operand size increases, linear arrays grow at a rate equal to the square of the operand size because the number of rows in the array is equal to the width of multiplicand.

C.Baugh-Wooley Multiplier & Brawn Multiplier

Brawn multiplier is shown in figure 3.

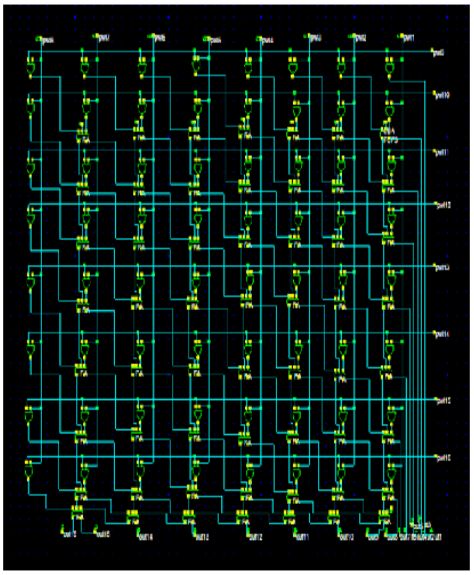

Figure 3. *Brawn multiplier*

A Brawn multiplier is an enhanced version of the Baugh-Wooley multiplier. It is designed to allow for the multiplication of both signed and unsigned operands, which are represented in the 2's complement number systems. The Figure 4: Baugh-Wooley proposes a single modification to 2's complement addition to obtain a simple signed multiplier array. It uses inputs A and B which are n bit operands, so their product is a 2n-bit number. Consequently the most significant weight is 2n-1, and the first term is taken in to account by adding a 1 in the most significant cell of the multiplier. The conventional Baugh-Wooley multiplier is shown in figure 4.

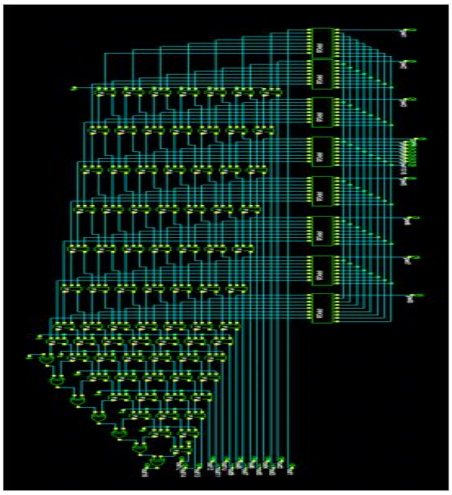

Figure 4. *Baugh-Wooley multiplier*

Table1. *Comparisons between multipliers*

Multipliers	Power (mw)	Delay (ns)	P D P (pj)
Radix-8	2.034	12.61	25.648
Brawn	2.107	14.09	29.687
Bawgh-Wooley	2.193	12.18	26.710

4. CONCLUSION AND FUTURE WORK

The adder cell was designed using a modified CPL technique. The 1-bit adder cell was implemented in radix-8, Baugh-Woolley and Brawn multipliers. The simulations results are calculated for five multiplications which are taken randomly. The proposed Radix-8 Multiplier may be used in DSP applications because it gives better performance in terms of power, delay and PDP. Even though delay

is more than Brawn multiplier the power and PDP is less than other multipliers. The proposed adder based multiplier can be used in high speed application because of its less power dissipation.

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