A Novel 128-Bit QCA Adder

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Abstract: *A new 128-bit adder designed in QCA was presented. It achieved speed performances higher than all the existing. QCA adders, with an area requirement comparable with the cheap RCA and CFA demonstrated. The novel adder operated in the RCA fashion, but it could propagate a carry signal through a number of cascaded MGs significantly lower than conventional RCA adders. In addition, because of the adopted basic logic and layout strategy, the number of clock cycles required for completing the elaboration was limited. As transistors decrease in size more and more of them can be accommodated in a single die, thus increasing chip computational capabilities. However, transistors cannot get much smaller than their current size. The quantum-dot cellular automata (QCA) approach represents one of the possible solutions in overcoming this physical limit, even though the design of logic modules in QCA is not always straightforward.*

Index Terms: *Adders, nano-computing, quantum-dot cellular automata (QCA)*

1. INTRODUCTION

Quantum-dot cellular automata (QCA) is an attractive emerging technology suitable for the development of ultra dense low-power high-performance digital circuits. For this reason, in the last few years, the design of efficient logic circuits in QCA has received a great deal of attention. Special efforts are directed to arithmetic circuits, with the main interest focused on the binary addition that is the basic operation of any digital system. Of course, the architectures commonly employed in traditional CMOS designs are considered a first reference for the new design environment. Ripple-carry (RCA), carry look-ahead (CLA), and conditional sum adders were presented in. The carry-flow adder (CFA) shown in was mainly an improved RCA in which detrimental wires effects were mitigated. Parallel-prefix architectures, including Brent–Kung (BKA), Kogge–Stone, Ladner–Fischer, and Han–Carlson adders, were analyzed and implemented in QCA. Recently, more efficient designs were proposed for the CLA and the BKA, and for the CLA and the CFA. In this brief, an innovative technique is presented to implement high-speed low-area adders in QCA. Theoretical formulations demonstrated for CLA and parallel-prefix adders are here exploited for the realization of a novel 2-bit addition slice. The latter allows the carry to be propagated through two subsequent bit-positions with the delay of just one majority gate (MG). In addition, the clever top level architecture leads to very compact layouts, thus avoiding unnecessary clock phases due to long interconnections.

An adder designed as proposed runs in the RCA fashion, but it exhibits a computational delay lower than all state-of the- art competitors and achieves the lowest area-delay product (ADP). The rest of this brief is organized as follows: a brief background of the QCA technology and existing adders designed in QCA is given in Section II, the novel adder design is then introduced in Section III, simulation and comparison results are presented in Section IV, and finally, in Section V conclusions are drawn.
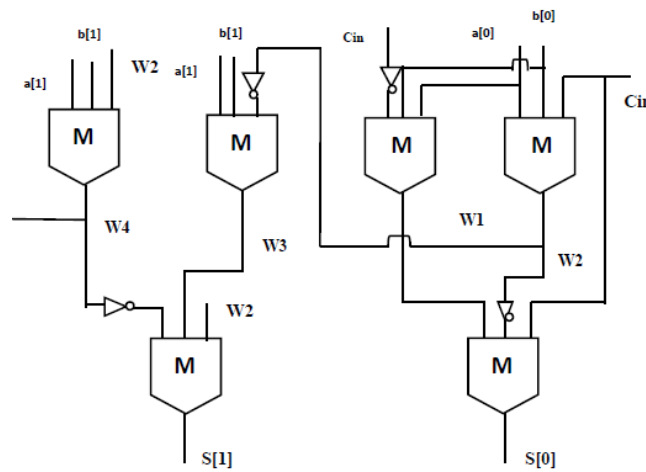
Fig 1. *Novel 2-bit basic module*

2. BACKGROUND

A QCA is a nanostructure having as its basic cell a square four quantum dots structure charged with two free electrons able to tunnel through the dots within the cell. Because of Coulombic repulsion, the two electrons will always reside in opposite corners. The locations of the electrons in the cell (also named polarizations *P)* determine two possible stable states that can be associated to the binary states 1 and 0.

Although adjacent cells interact through electrostatic forces and tend to align their polarizations, QCA cells do not have intrinsic data flow directionality. To achieve controllable data directions, the cells within a QCA design are partitioned into the so-called clock zones that are progressively associated to four clock signals, each phase shifted by 90°. This clock scheme, named the zone clocking scheme, makes the QCA designs intrinsically pipelined, as each clock zone behaves like a D-latch. QCA cells are used for both logic structures and interconnections that can exploit either the coplanar cross or the bridge technique. The fundamental logic gates inherently available within the QCA technology are the inverter and the MG. Given three inputs *a*, *b,* and *c*, the MG performs the logic function reported in (1) provided that all input cells are associated to the same clock signal clk*x* (with *x* ranging from 0 to 3), whereas the remaining cells of the MG are associated to the clock signal clk*x*+1
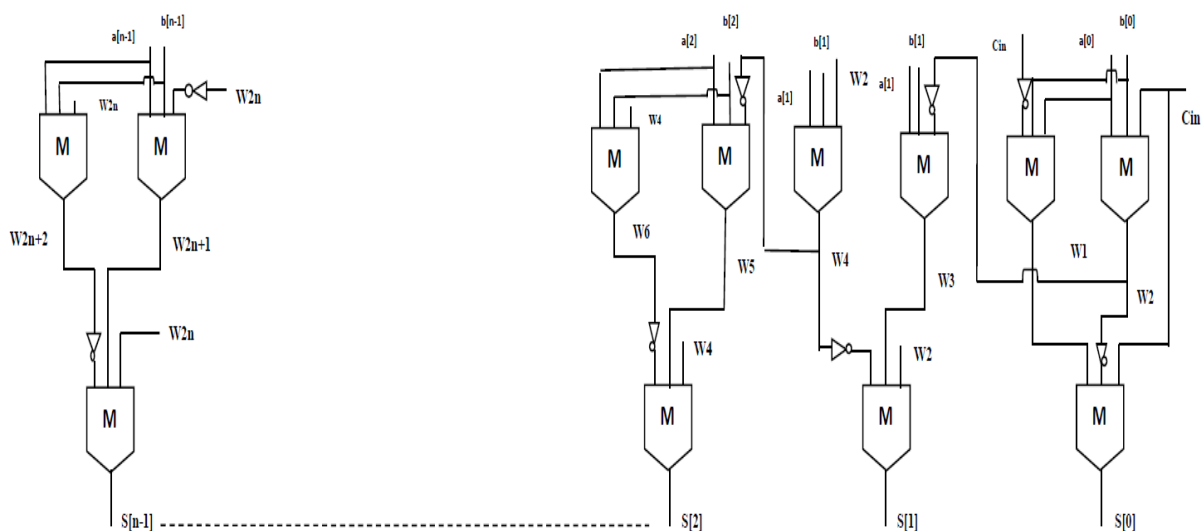
$$M(abc) = a \cdot b + a \cdot c + b \cdot c. \tag{1}$$

Fig 2. *Novel n-bit adder*

Several designs of adders in QCA exist in literature. The RCA [11], [13] and the CFA [12] process *n*-bit operands by cascading *n* full-adders (FAs). Even though these addition circuits use different

topologies of the generic FA, they have a carry-in to carry-out path consisting of one MG, and a carry-in to sum bit path containing two MGs plus one inverter. As a consequence, the worst case computational paths of the *n*-bit RCA and the *n*-bit CFA consist of $(n+2)$ MGs and one inverter. A CLA architecture formed by 4-bit slices was also presented. In particular, the auxiliary propagate and generate signals, namely

$p_i = a_i + b_i$ and $g_i = a_i . b_i$, are computed for each bit of the operands and then they are grouped four by four. Such a designed *n*-bit CLA has a computational path composed of $7+4\times(\log_4 n)$ cascaded MGs and one inverter. This can be easily verified by observing that, given the propagate and generate signals (for which only one MG is required), to compute grouped propagate and grouped generate signals; four cascaded MGs are introduced in the computational path. In addition, to compute the carry signals, one level of the CLA logic is required for each factor of four in the operands word-length. This means that, to process *n* bit addends, $\log_4 n$ levels of CLA logic are required, each contributing to the computational path with four cascaded MGs. Finally, the computation of sum bits introduces two further cascaded MGs and one inverter. The parallel-prefix BKA demonstrated exploits more efficient basic CLA logic structures. As its main
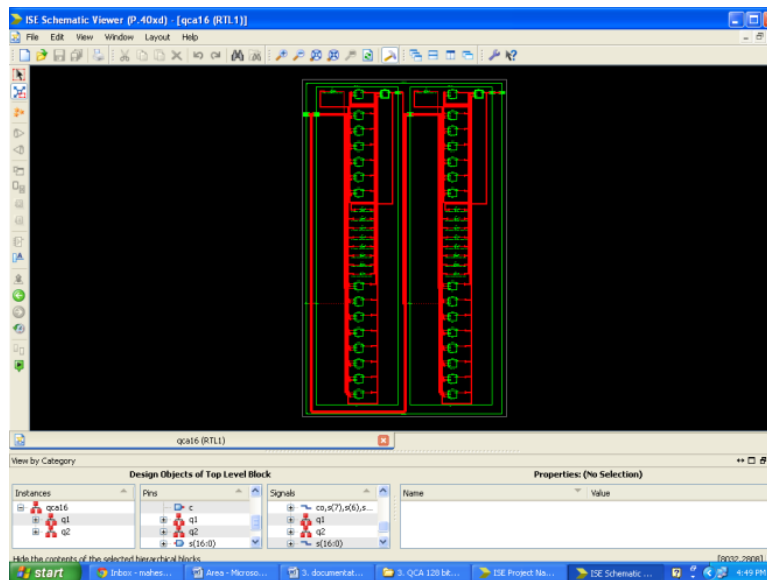

Novel 16-bit adder

Advantage over the previously described adders, the BKA can achieve lower computational delay. When *n*-bit operands are processed, its worst case computational path consists of $4\times\log_2 n - 3$ cascaded MGs and one inverter. Apart from the level required to compute propagate and generate signals, the prefix tree consists of $2 \times \log_2 n - 2$ stages. From the logic equations provided, it can be easily verified that the first stage of the tree introduces in the computational path just one MG; the last stage of the tree contributes with only one MG; whereas, the intermediate stages introduce in the critical path two cascaded MGs each. Finally, for the computation of the sum bits, further two cascaded MGs and one inverter are added. With the main objective of trading off area and delay, the hybrid adder (HYBA) described combines a parallelprefix adder with the RCA. In the presence of *n*-bit operands, this architecture has a worst computational path consisting of $2 \times \log_2 n + 2$ cascaded MGs and one inverter. When the methodology recently proposed was exploited, the worst case path of the CLA is reduced to $4 \times [\log_4 n] + 2 \times [\log_4 n] - 1$ MGs and one inverter. The above-mentioned approach can be applied also to design the BKA. In this case the overall area is reduced with respect to, but maintaining the same computational path. By applying the decomposition method demonstrated, the computational paths of the CLA and the CFA are reduced to $7 + 2 \times \log_4(n/8)$ MGs and one inverter and to $(n/2) + 3$ MGs and one inverter, respectively.

3. NOVEL QCA ADDER

To introduce the novel architecture proposed for implementing ripple adders in QCA, let consider two *n*-bit addends $A = a_{n-1}, \ldots, a_0$ and $B = b_{n-1}, \ldots, b_0$ and suppose that for the *i* th bit position (with *i* $= n - 1, \ldots, 0$) the auxiliary propagate and generate signals, namely $p_i = a_i + b_i$ and
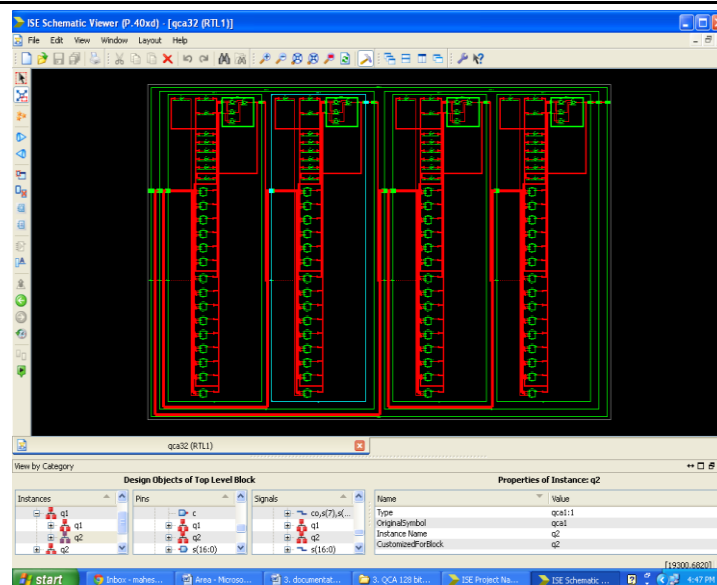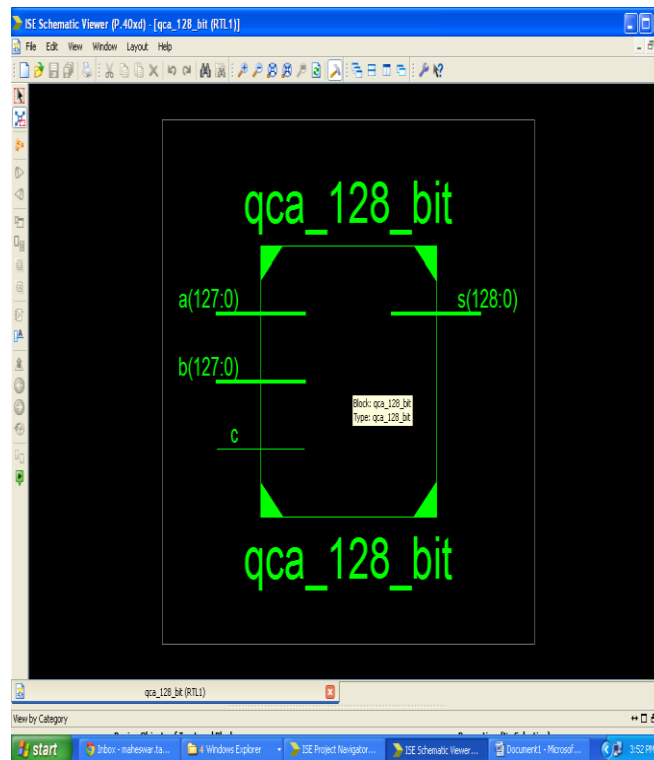
Novel 32-bit adder
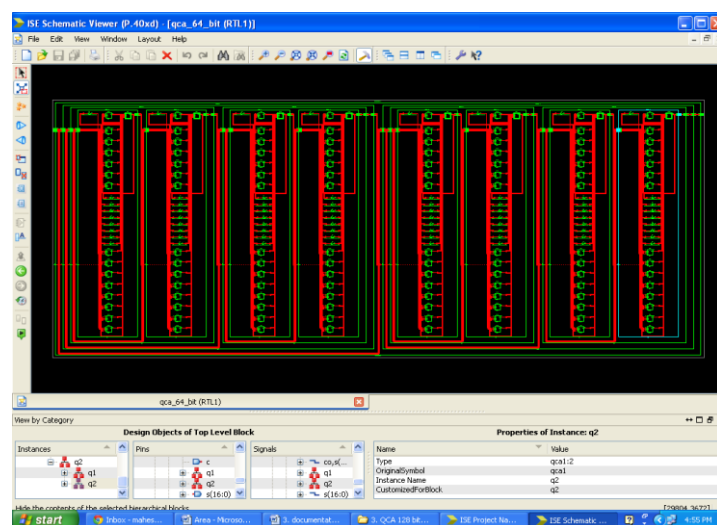
Novel 64-bit adder

$g_i = a_i \cdot b_i$, are computed c_i being the carry produced at the generic $(i-1)$th bit position, the carry signal $ci+2$, furnished at the $(i+1)$th bit position, can be computed using the conventional CLA logic reported. The latter can be rewritten as given in (3), by exploiting Theorems 1 and *2* demonstrated. In this way, the RCA action, needed to propagate the carry c_i through the two subsequent bit positions, requires only one MG. Conversely, conventional circuits operating in the RCA fashion, namely the RCA and the CFA, require two cascaded MGs to perform the same operation. In other words, an RCA adder designed as proposed has a worst case path almost halved with respect to the conventional RCA and CFA. Equation (3) is exploited in the design of the novel 2-bit module shown in Fig. 1 that also shows the computation of the carry $c_{i+1} = M(p_i g_i c_i)$. The proposed *n*-bit adder is then implemented by cascading *n/*2 2-bit modules as shown in Fig. 2(a). Having assumed that the carry-in of the adder is $c_{in} = 0$, the signal p_0 is not required and the 2-bit module used at the least significant bit position is simplified.

It must be noted that the time critical addition is performed when a carry is generated at the least significant bit position and then it is propagated through the subsequent bit positions to the most significant one. In this case, the first 2-bit module computes c_2, contributing to the worst case computational path with two cascaded MGs. The subsequent 2-bit modules contribute with only one MG each, thus introducing a total number of cascaded MGs equal to *(n − 2)/2*. Considering that further two MGs and one inverter are required to compute the sum bits, the worst case path of the novel adder consists of *(n/2) + 3* MGs and one inverter.
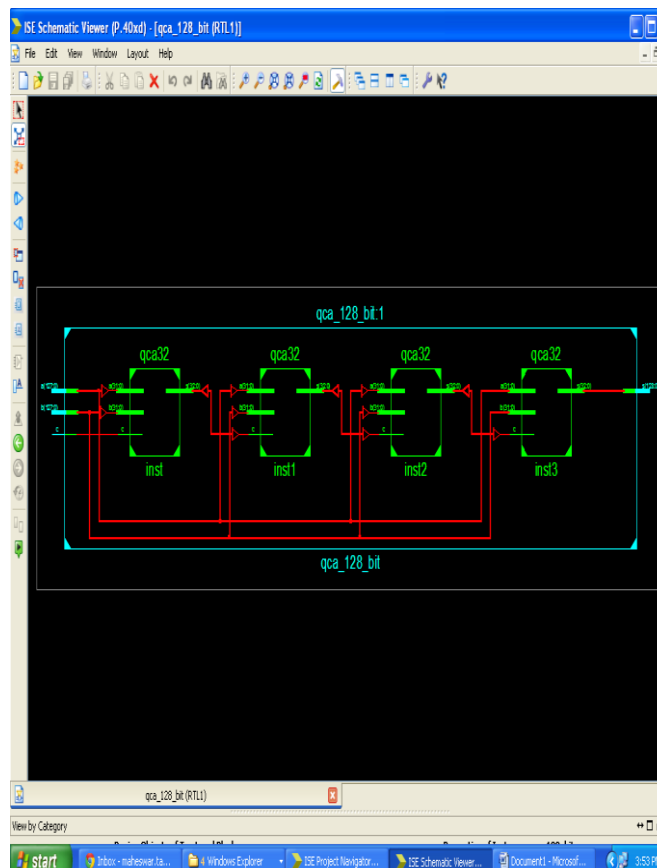
4. RESULTS

The proposed addition architecture is implemented for several operands word lengths using the QCA Designer tool adopting the same rules and simulation settings used.
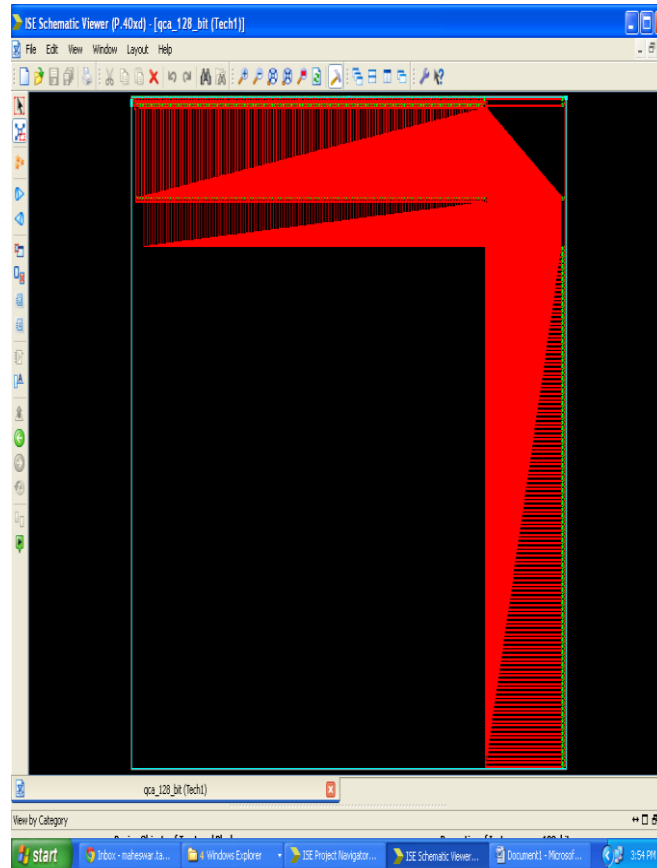
Block Diagram

RTL Schematic

Technology Schematic

Design Summary

Simulation Output

5. CONCLUSION

A new adder designed in QCA was presented. It achieved speed performances higher than all the existing QCA adders, with an area requirement comparable with the cheap RCA and CFA demonstrated. The novel adder operated in the RCA fashion, but it could propagate a carry signal through a number of cascaded MGs significantly lower than conventional RCA adders. In addition, because of the adopted basic logic and layout strategy, the number of clock cycles required for completing the elaboration was limited. A 128-bit binary adder designed as described in this brief.

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