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Implementation of Low Power 32 Bit ETA Adder

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Abstract: *In modern VLSI technology, an emerging concept is adapted in VLSI design and test, High Speed and novel low power Adder is proposed. The proposed adder achieves tremendous improvements in both the speed performance and power consumption. Existing adder designs have shown substantial advantages in improving many of these operational features. However, the error characteristics of the approximate adders still remain an issue that is not very well understood. A simulation-based method requires both programming efforts and a time-consuming execution for evaluating the effect of errors. This method becomes particularly expensive when dealing with various sizes and types of approximate adders. When conventional counter parts are compared to the proposed adder is able to attain drastic improvement in the Power-Delay Product. In digital signal processing systems that can improve speed performance with the help of this proposed adder. Delay and power are compared for various adders like RCA, CSK CSL and ETA. It is found the proposed adder PDP is noted to be 86.46%, 77.72%, 77.28%, and 71.89% better than the CSL,CSK ,RCA and ETA respectively*

Keywords: *Adders, digital signal processing (DSP), error tolerance, high-speed integrated circuits, low-power design, VLSI*

1. INTRODUCTION

Very-Large-Scale Integration (VLSI) is the method of designing integrated circuit by combining thousands of transistors into a single chip. VLSI began in the 1970s when communication technologies and complex semiconductors were being developed. The microprocessor is a Very-Large-Scale-Integration device.Success have to wait after WWII, during the attempt to better the silicon crystals and the germanium crystals for use as a detectors to improves the fabrication and to understand the quantum states of carriers in semiconductors. With the help of the less and good transistor at hands, engineers of the 1950s saw the different number of advanced circuits. If the elements of the computer we also very long, the signals couldn't pass through as enough through the circuit, hence making the computer is slow to be effective. Jack kilby at Texas found a result to this problem in 1958. By manufacturing all the important blocks out of the same part of material and adding the new metal needed to connect them as a layer on top of the material, there was no necessary for discrete parts. The circuits may be made to smaller and the developing method could automation. The first chip having two transistor, with adequate shape having more transistors, and high operations were implemented with in time. The very first integrated circuit manufactured by few devices only, having ten diodes, transistors, resistors and capacitors, making it possible to develop more or one logic gates on a si device.The famous Moore‘s Law provides us an consequence trend in the development of integrated circuit technology. According to Moore‘s Law, the number of transistors that can be inexpensively on an integrated circuit will doubled every two years. This has continued about half a century and is not to stop in at least next decade.However, the distinctive size of the complementary metal-oxide-semiconductor (CMOS) approaches the deep sub-micron —nano-scale, significant challenges to sustaining Moore‘s Law have emerged. Two of these challenges are the

impact of noise and achieving low-power consumption. However, the requirement for increasing noise immunity contradicts with the traditional methodology to achieve low-power consumption, which is addressed by voltage scaling, as reducing the voltage level may greatly degrade the noise immunity of the circuits. Under this circumstance, a new technology, Probabilistic CMOS (PCMOS) technology, was proposed.

1.1 Conventional Adders:

Adder is the most basic and important cell in most computational systems. It is usually the dominant factor in determining the overall performance of the whole system. Arithmetic design blocks play a crucial role in the digital and mixed-signal systems. The bottleneck of digital signal processing and many other digital systems is arithmetic blocks where addition and multiplication operations are the core units. As the VLSI technology reduces to nanometre size devices, power dissipation reduces and device speeds increase every year. However, silicon technology is reaching its physical limits, where the design sizes already have reached the atomic levels. In this, alternative circuit design techniques are proposed for arithmetic systems that can help designing analog friendly circuits; or increase performance with lower power consumption. Addition of numbers is the most basic operation of all arithmetic systems, such as subtraction, multiplication and division. In the basic addition structure, the addition time is proportional to the numbering systems to be added since the next output digit depends on previous carry-out of each digit. This causes an unacceptable delay for many systems especially when the word-length of the input operands is high. Therefore, carry signal propagation must be eliminated in the arithmetic circuits. There have been various techniques developed for breaking the long carry chains of the arithmetic circuits. Now we discuss different adders with how carry is propagating. The addition of two binary bits is performed by half adder circuit that means in order two add two bits according to the some specified manner is called Half Adder (HA).in another case in order to sum to or more i.e. three bits only we can use Full Adder(FA) circuit, It is a combination of two HA's also. The basic building block of this circuit also will be provided in the following way

2. ADDER TYPES

In this concept we can explain about the different types of adders and explanation of their characteristics and their performances. Each adder having different power, delay and area depending upon their architecture as following manner.

2.1 Ripple Carry Adder

The block diagram of ripple carry adder is given by

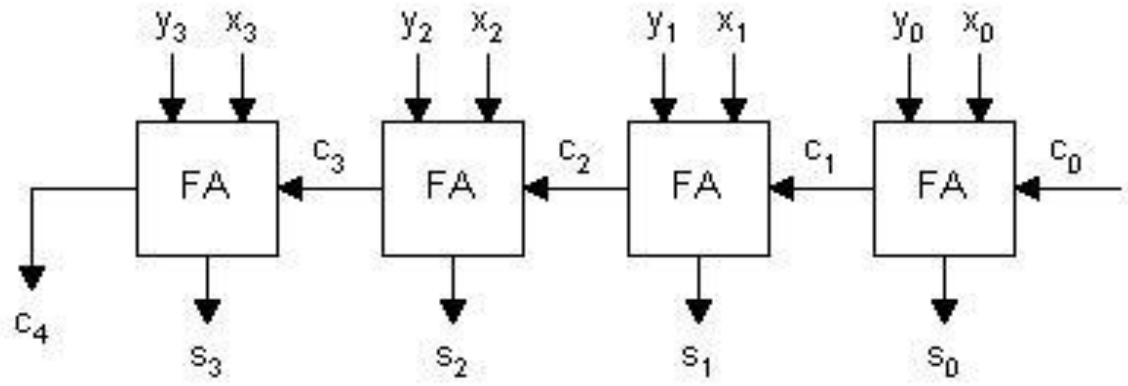

Figure 1. *Ripple Carry Adder*

The critical path delay for this adder can be designed as

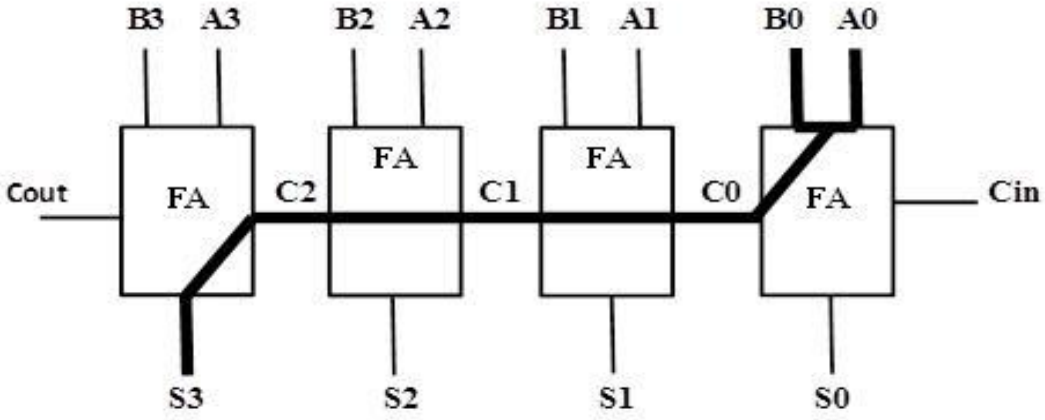

Figure 2. *Critical path delay*

2.2 Carry Look Ahead Adder

The block diagram given in the following implementation

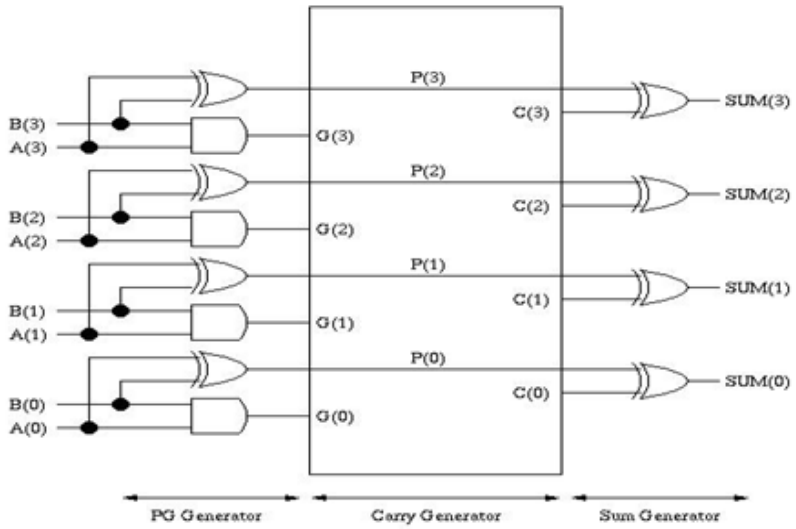

Figure 3. *Carry look ahead adder*

Here generator of sum given by

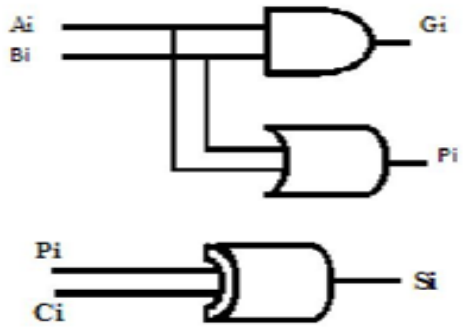

Figure 4. *Sum generator*

The Figure 4 shows the generator of carry is as in following manner

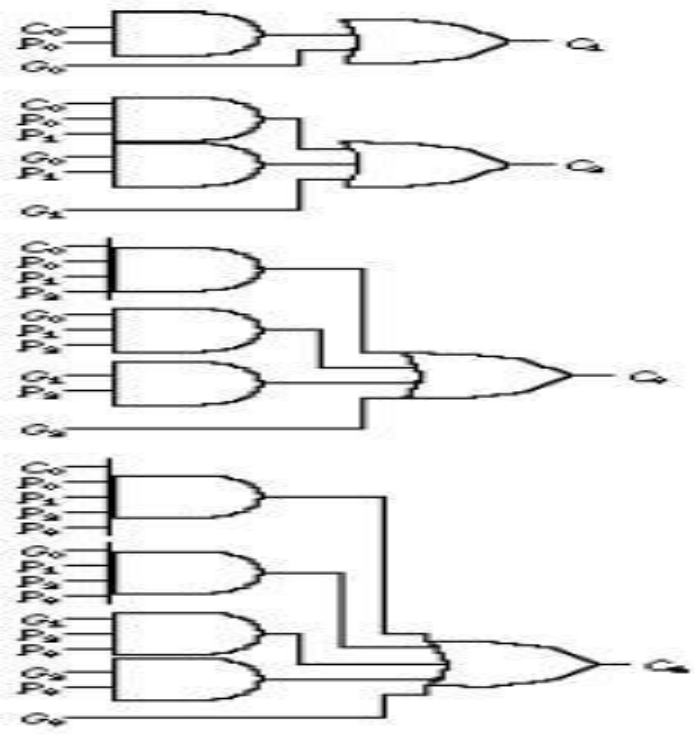

Figure 5. *Carry Generator*

2.3 Hierarchical Look Ahead Adder

As increase of n, the size of block to be limited as and ripple delay accumulates. It is no longer impractical to standard look-ahead method. Instead of this two level carry look-ahead adder is used. In this design, the CLAs generate the sums first as well as generate and propagate signals at second level as in below figure

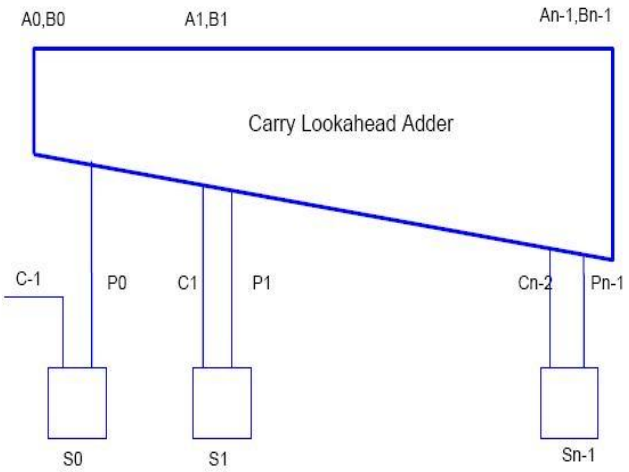

Figure 6. *Hierarchical Carry look-ahead depth*

2.4 Carry Select Adder:

A CSA can be implemented by the single ripple carry adder and as well as an add-one circuit to reduce the power and delay but with speed penalty. A fast and extremely high performance adder which is having an excellent selection of sum and ripple carry which is multiple radix is described in the following block diagram

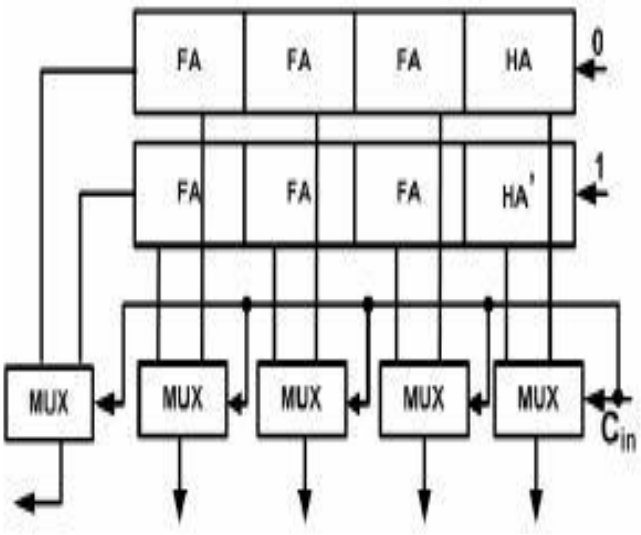

Figure 7. *Conventional carry-select adder*

The selection of the true, sub sum from of the adder section is depending on whether or not actually is a carry into the adder section. In the above block diagram muxes and full adders as well as carry are an important parts.

2.5 Error Tolerant Adder

Need For Eta:

A designer can either develop faster electronic materials and circuitry having slow components into faster, for more efficient systems. In recent methods, increased speed is obtained by combining the electronic devices into more complex structures. It describes fast and low power digital adders that abruptly reduce the need for carry propagation, without requiring an excessive of additional hardware.

ETA is defined as a digital adder that does not always yield correct results but is still usable in some systems by generating ―acceptable results. In an ETA, errors may occur at the output of the adder due to some internal or external factors. According to the definition given above, the ETA is a broad category of adders.

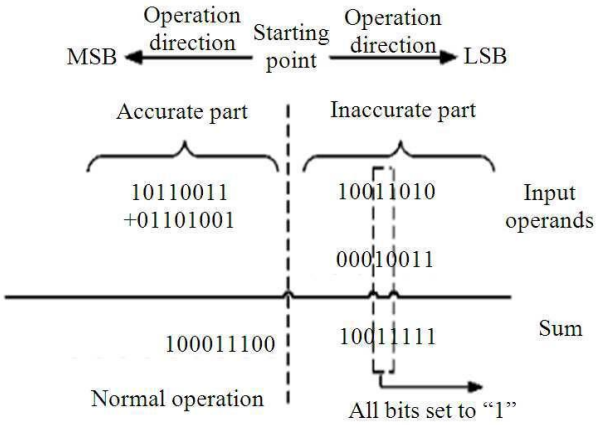

Figure 8. *Procedure of Addition Arithmetic*

There can be numerous ways to implement an ETA. In this chapter, methodologies that serve to provide an investigation in this emerging research area are presented. In the proposed designs, the errors are caused by special addition mechanisms and circuit structures. Prior to discussing on the ETA, the exact definitions and explanations. The hardware implementation is given by

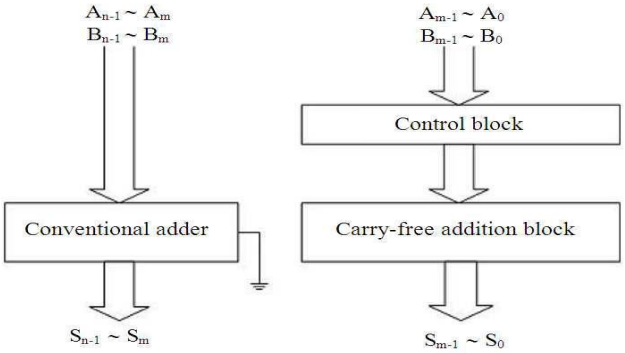

Figure 9. *Hardware implementation of ETA*

The schematic diagram of modified xor gate is given by

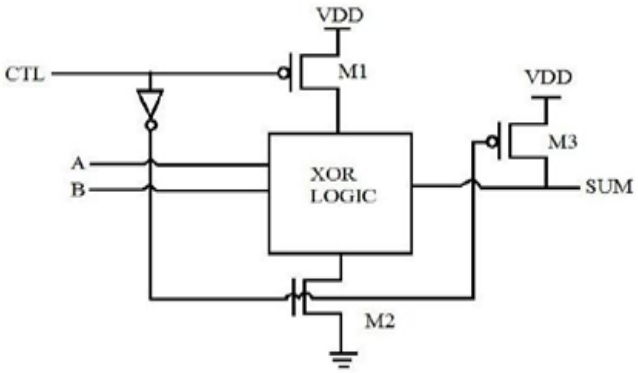

Figure 10. *Schematic diagram of modified XOR gate*

The overall structure of control block and carry free addition block is given by the following manner

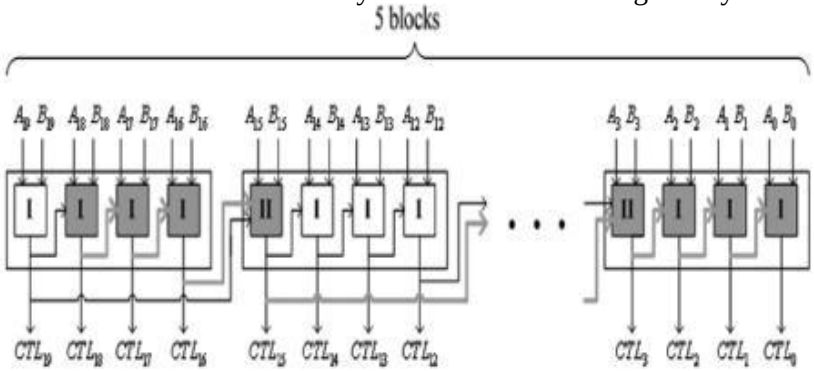

Figure 11. *Overall structure of control block*

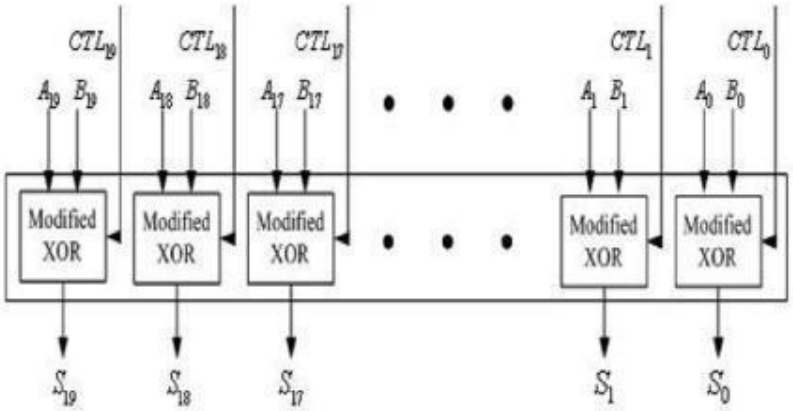

Figure 12. *overall structure of carry free addition block*

2.6 Proposed Low Power 32-Bit ETA adder:

Proposed Addition Arithmetic

In a general adder circuit, the delay is attributed to the carry propagation along the critical path, from the LSB to the MSB. Figure4.1 the two 32-bit input operands—10010101101101011101011101010101 and—01101010110100111111011011010110 are added directly. So, the sum bits generated by using control block.

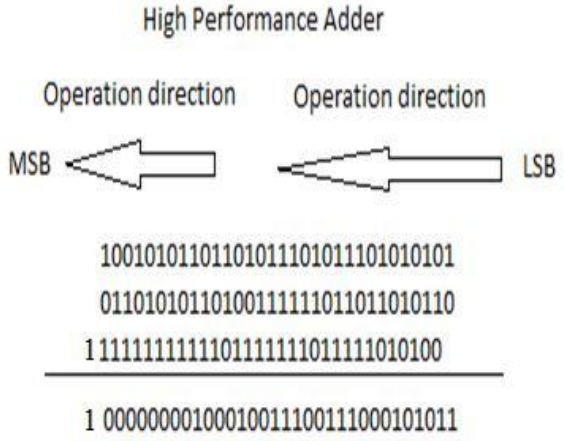

Figure 13. *proposed addition arithmetic*

3. HARDWARE IMPLEMENTATION

The hardware implementation is given by the above figure 4.2.The most straight forward structure consists of 2 blocks: a modified carry free addition and control block.

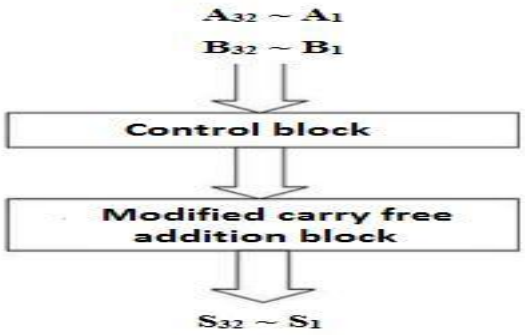

Figure 14. *Hardware implementation of proposed adder*

The second block to implement the high speed carry signals and fed to modified free carry addition block.So the performance is increased in the proposed adder since carry signals are generated in prior with high speed. The proposed high performance adder gives 100% accuracy. The diagram of the modified 3input xor gate is presented by figure 15.

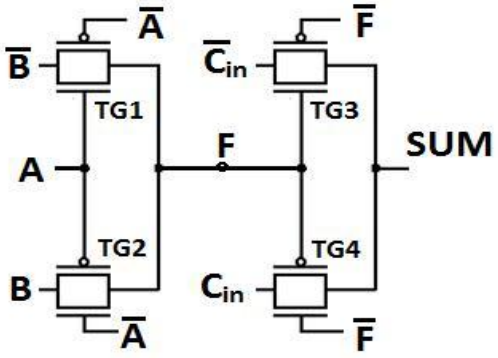

Figure 15. *Modified 3-input XOR*

The modified 3 input XOR gate is used in the modified carry free addition block. It has 16 transistors as shown in figure 15. Where, as in the ETA the modified XOR gate consist of 27 transistors as shown in figure.So the proposed carry free addition block has less number of transistors compared to the existing carry free addition block. The modified free carry addition block is implemented by using 32bit changed three input xor gates as shown in figure 14. Each of modified 3 input XOR gate generates a sum bit.The use of this block is to generate carry signals. It is made up of 32 modified 4x1 multiplexers (MUXs) as shown in figure 15. The schematic implementation of modified 4x1 mux is explained in figure 14. The all inputs of modified 4x1 MUX are 0, C_i and 1. Where C_i is i^{th} stage carry signal and output is C_{i+1}. Where C_{i+1} is $(i+1)^{th}$ stage carry signal. The operation of modified 4x1 MUX is explained in Table 1

Table 1. *The operation of 4x1 MUX*

INPUTS	SELECTON LINES		ON TRANSMISSIN GATES	OFF TRANSMISSION GATES	4x1 MUX OUTPUT
	A	B			
0	0	0	TG1, TG3, TG5	TG2, TG4, TG6	0
C_i	0	1	TG1, TG3, TG6	TG2, TG4, TG5	C_i
Ci	1	0	TG2, TG4, TG5	TG1, TG3, TG6	Ci
1	1	1	TG2, TG4, TG6	TG1, TG3, TG5	1

4. APPLICATION OF HIGH PERFORMANCE ADDER IN DSP

4.1 Applications of High Speed Adders

After introducing the algorithms, mathematical properties, and schematic implementations, the question naturally comes to the application-level. The proposed HPA‘s have shown their outstanding performance in both power and speed.

4.2 Application of FFT in DSP

The applications of DSP have penetrated into many different areas. Because of its importance in today‘s electronic technology, how to enhance the performance of DSP systems (i.e., has higher speed and consumes fewer resources) has become a very important issue.FFT is the basis and one of the most important functions of DSP. In DSP applications, there are usually five processing steps: firstly, the analog signals sampled from outside world are converted to digital signals; secondly, the digital signals are transformed from time/space domain (For the signals like speech signal, it is time domain; for the signals like image signal, it is space domain.) to the frequency domain using FFT function; thirdly, spectral analysis and many kinds of signal processing, such as filtration and signal convolution, are conducted to the signals in the frequency domain; fourthly, the processed signals are transformed from domain of frequency to space using inverse FFT function; lastly, the digital signals are converted back to analog signals

4.3 Digital Image Processing

The is taken as platform to illustrate the application of the HPA-based FFT, which leads to the application of the proposed HPA‘s. This information is an important role in every area of people‘s life.

5. SIMULATION RESULTS

We have designed and simulated High performance Adder (HPA) in HSPICE tool and compared with other adders and explained in below result.

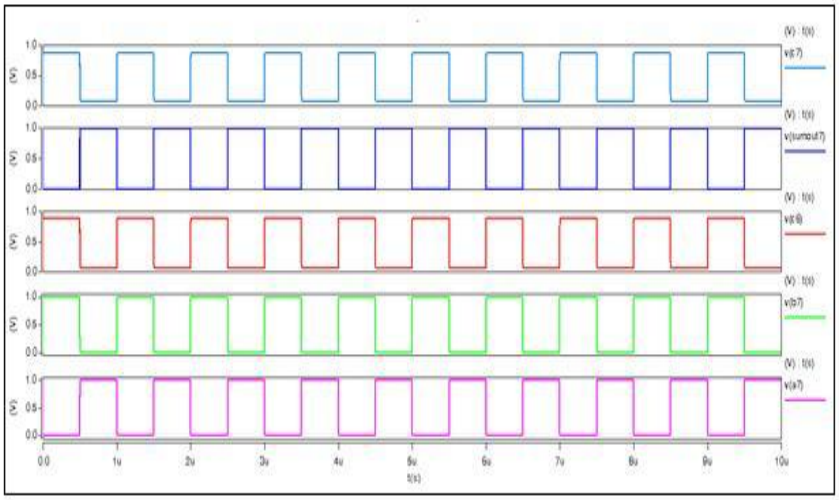

Figure 16. *Simulation result for proposed HPA*

Average power of proposed HPA:

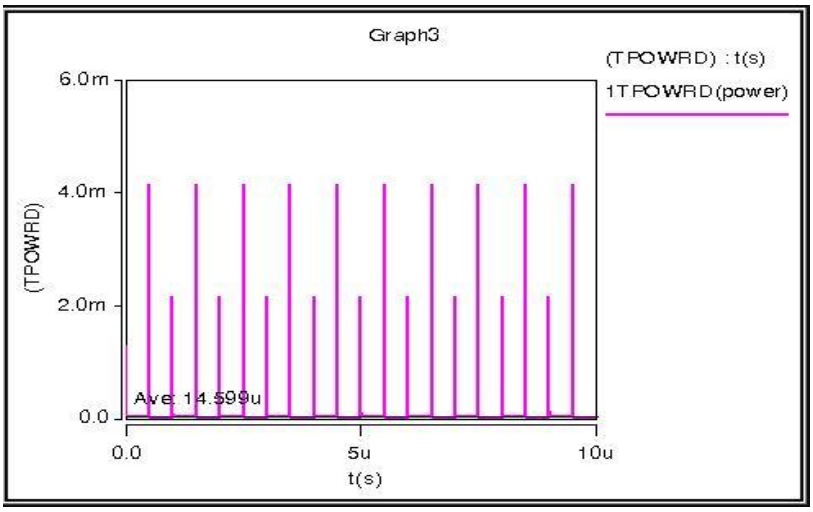

Figure 17. *Output waveforms for average power of proposed HPA*

Delay of Proposed HPA:

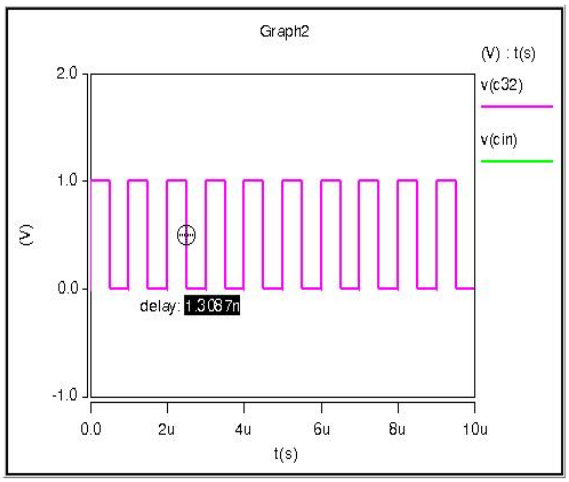

Figure 18. *Output waveform for Delay of Proposed HPA*

By analyzing the statistical report, the proposed High performance adder (HPA) provides high speed and consume less power with less number of transistors.

6. COMPARISION OF DIFFERENT ADDERS

Table 2. *Comparision of different adders*

Name of the adder	Power(µw)	Delay(ns)	Power-Delay Product (PDP)	Transistor Count
Ripple Carry Adder	27.25	5.18	158.32	896
Carry Skip Adder	38.13	2.25	85.79	1442
Carry Select Adder	42.92	1.96	84.26	2100
Error Tolerant Adder	31.63	2.15	68.00	924
High Performance Adder	14.599	1.3087	19.105	904

7. CONCLUSION

In this project, the concept of high performance adder is introduced in VLSI design. A novel type of high performance adder, which attains good accuracy for significant power saving and performance improvement. Extensive comparisons with conventional digital adders showed that the proposed HPA outperformed the conventional adders in both power consumption and speed performance. The potential applications of the HPA fall mainly in areas where there is requirement on accuracy, super low power consumption and high-speed performance are more important.

8. FUTURE SCOPE

This project has started a new direction of digital integrated circuit and system design. On the road of exploring in this new direction, there are a lot more work that can and need to be done. The design can be extended from adder to other digital circuits and eventually the whole digital system. The concept of HPA has been proven to be feasible by employing it in digital image processing. It is therefore logical to extend this concept to other digital circuits such as the multiplier, and to a whole DSP system.

The design can be extended from the Application Specific Integrated Circuit (ASIC) implementation to the Field Programmable Gate Array (FPGA) implementation. FPGA is becoming more and more popular in digital system design because of its many advantages over the ASIC. Hence, employing the concept of high speed of operation in FPGA implementation may also be a valuable work. Although there are still a lot of work needed to be done in the future, this project has already provided a good start in this completely new and very promising area.

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