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Single Phase Bridgeless SEPIC Converter with High Power Factor

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Abstract: *Conventional Power Factor Correction circuits consists of a diode bridge rectifier and a DC-DC converter. Diode bridge rectifier at the input side leads to severe conduction losses and thereby efficiency of the converter is reduced. In an effort to achieve high efficiency AC/DC power supplies, bridgeless converters that eliminate the bridge diodes have recently become popular. In bridgeless converter, conduction losses are reduced as the number of simultaneously conducting components on input current path is comparatively lesser than conventional converters. In this paper a bridgeless Single Ended Primary Inductance Converter (SEPIC) PFC is presented which has lesser number of components, less conduction losses and high power factor.*

Keywords: *Bridgeless converter, Single Ended Primary Inductance Converter (SEPIC), Power Factor Correction (PFC)*

1. INTRODUCTION

Power factor is defined as the ratio of real power to apparent power and its value ranges from 0 to 1. When the voltage and current waveforms are in phase, the power factor is said to be unity. A non-corrected power supply with a typical power factor equal to 0.65 will draw approximately 1.5 times greater input current than a power factor corrected supply (pf = 0.99) for the same output loading. When voltage and current are in phase with each other in an AC circuit, the electrical energy drawn from the mains is fully converted into another form of energy in the loads and the power factor is unity. As the power factor drops, the system becomes less efficient. When the power factor is not equal to 1, the current waveform does not follow the voltage waveform. This results not only in power losses, but may also cause harmonics that travel down the neutral line and disrupt other devices connected to the line. The closer the power factor is to unity, lesser the current harmonics, since all the power is contained in the fundamental frequency.

The equipment connected to an electricity distribution network usually needs some kind of power conditioning, typically rectification, which produces a non-sinusoidal line current due to the non-linear input characteristic. Diode rectifiers convert AC input voltage into DC output voltage in an uncontrolled manner and are widely used in relatively low power equipment, such as electronic equipment and household appliances. In both single and three-phase rectifiers, a large filtering capacitor is connected across the rectifier output to reduce the ripple in the DC. As a consequence, the line current is non sinusoidal. In most of these cases, the amplitude of odd harmonics of the line current is considerable with respect to the fundamental. Line current harmonics have a number of undesirable effects on both the distribution network and consumers. The presence of nonlinear loads leads to high harmonics and results in poor power factor at the input side and also poor power quality.

In order to ensure good quality power supply various international agencies have proposed different standards such as IEC 1000-3-2, EN 61000-3-2, IEEE 519-1992 etc. These standards gives

recommended practices and requirements for harmonic control in electrical power system for both individual consumers and utilities. So to comply with the recommended standards it is necessary to use suitable power factor correction technique to reduce the harmonic distortion and improve the power factor. Power factor Correctors (PFC) are broadly classified as Passive PFC and Active PFC. Passive PFC uses only passive elements such as inductor and capacitor. Even though passive PFC's are simple and robust, the circuit is bulky and expensive. Also it suffers from poor dynamic response, shape of input current depends on the load and is less efficient.

Power supplies with active power factor correction (PFC) techniques are becoming increasingly popular for many types of electronic equipment to meet harmonic regulations and standards. In active PFC active switches are used in conjunction with reactive elements and provides more efficient solution for power factor correction. Also the output voltage is controllable. In active power factor correction techniques the switching takes place at high frequency and shapes the input current as close as possible to a sinusoidal waveform which is in phase with input voltage

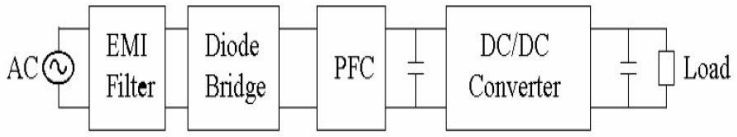


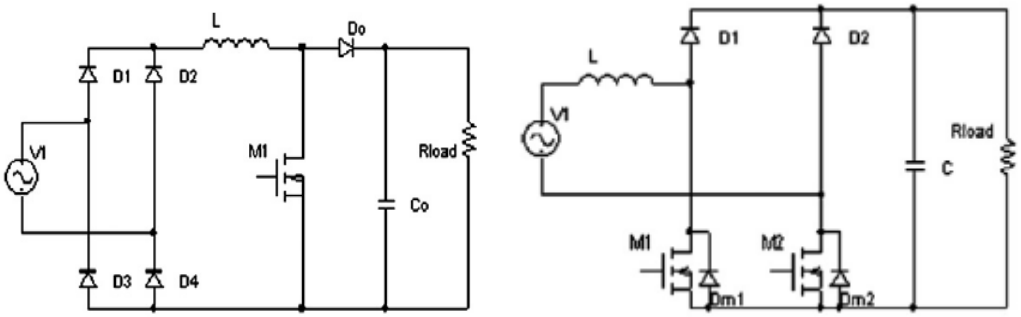
Figure 1. *Block diagram of power supply with Active PFC*

The active power factor correction (PFC) [1] circuits are widely used to effectively draw the energy from the mains via an AC to DC converter. Conventional Power Factor Correction circuits utilize a diode bridge rectifier and a DC-DC converter at the front end [2]. Any DC-DC converters can be used for this purpose depending on the requirement. Commonly used converter for Power Factor Correction circuits are boost converters because of its low cost, high performance and simplicity. In Figure 2 a conventional Power Factor Correction circuit based on a boost DC-DC converter is shown.

However in conventional Power Factor Correction circuit's significant conduction loss are generated due the forward voltage drop across the diode bridge rectifier. The conduction losses across the bridge rectifier degrades the converter efficiency especially at low line input and high power applications. The converter efficiency can be improved by using a new topology called bridgeless circuits in which the diode bridge rectifier at the input side is eliminated. In bridgeless topology the lower part diode rectifier is replaced by two MOSFETs. In Figure 2(b) a bridgeless PFC circuit based on boost converter is shown. By comparing it with the conventional topology it is clear that the number of components in bridgeless topology is less and thereby lesser conduction losses and improved efficiency. Comparing the conduction path of conventional and bridgeless topology, at every moment, inductor current goes through two semiconductor devices in bridgeless topology, whereas in bridge topology it goes through three semiconductor devices.

The PFC circuits with boost converter at the DC-DC converter stage suffers from many drawbacks. The dc output voltage is always higher than the peak input voltage, size of EMI filter is larger, input–output isolation cannot be implemented easily, larger PFC inductance, the startup inrush current is high, and there is a lack of current limiting during overload conditions [3]-[4]. To overcome the problems associated with boost type PFC converters, especially in universal applications where the output voltage is lower than the input voltage the step up/down converters such as buck-boost, cuk, Single Ended Primary Inductance Converter (SEPIC) can be used. Among them a SEPIC converter offers several advantages as it can be used for both step up and step down operation. Also unlike the buck-boost and cuk topology, polarity of the output voltage is not reversed and thereby the control and

protection circuits can be easily implemented. Also if the input inductance is high, input current will have lesser ripples, thereby EMI filter requirements are reduced.



(a) (b)

Figure 2. *Schematic diagram of (a) conventional Boost Power Factor Correction circuit, (b) Bridgeless Boost Power Factor Correction circuit*

In this paper a bridgeless PFC circuit based on SEPIC converter is presented. The circuit diagram of the bridgeless PFC circuit is shown in Figure 3. The circuit is comparatively simpler than other bridgeless topologies [5]-[8]. The number of conducting components during each input-voltage cycle is less and the minimum number of output capacitor required is one. Also driving the MOSFETs gate terminal is simpler due to both source terminals of the MOSFETs are connected to a common node and no gate-driver circuit with isolation is required.

2. CIRCUIT OPERATION

In Figure 3 the circuit of bridgeless SEPIC PFC is shown. During positive half cycle, the switch S_1 is turned ON. The lower switch S_2 remains OFF. During the positive half cycle the diode D_{o1} conducts. The components that conduct are L_1, S_1, D_{S2}, C_{b1}, L_2, D_{O1}, C_o and R. During negative cycle, the upper switch S_1 is turned OFF and lower switch S_2 is turned ON. The components that conduct are L_1, D_{s1}, S_2, C_{b2}, L_3, D_{o2}, C_o and R. Thus during both the positive half cycle and the negative half cycle only eight components conducts which is comparatively less when compared to other power factor correction circuits. Here the converter is designed to operate in Discontinuous Conduction Mode (DCM). The converters operating in discontinuous mode offers several advantages, namely capability to operate as PFC is inherent, suitable for low power applications and lower component stress.

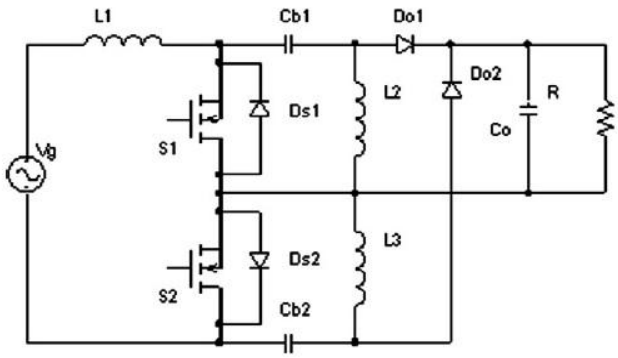


Figure 3. *Bridgeless SEPIC PFC circuit*

The circuit operation of the converter during positive half cycle and negative half cycle are similar. Operation of converter during positive half cycle consists of three subintervals MODE 1 (d_1T_S), MODE 2 (d_2T_S) and MODE 3 (d_3T_S). Operation of the converter during MODE 1, is shown in Figure

4. The upper MOSFET, S_1, is turned on, the current flows from the source, Vg, to the input inductor, L_1 and continue to S_1 and Ds_2 before completing the current path through Vg. The current through the inductor L_1 increases linearly and reaches its peak value, given by equation (1).

$$i_{L1peak} = \frac{V_g}{L_1}(d_1 T_s) \tag{1}$$

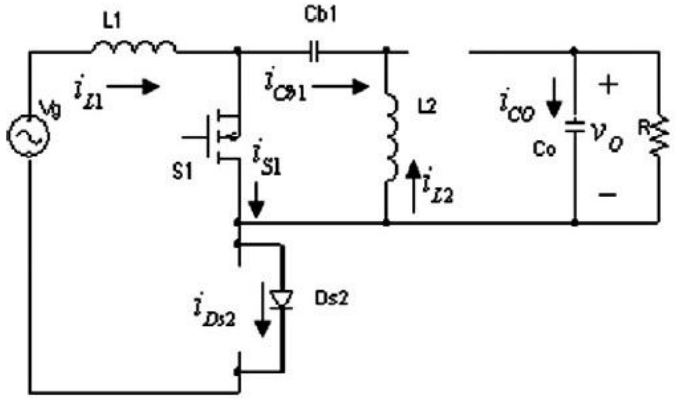


Figure 4. *Equivalent circuit during MODE 1 (d_1T_S)*

Where d_1 is the duty cycle. At the same time the second inductor, L_2 discharges its energy linearly to capacitor C_{b1}. A closed path for current flow is provided by MOSFET S_1, capacitor C_{b1} and inductor L_2. The net current flowing through switch S_1 during MODE 1 is the addition of the current through L_1 and L_2. The output diode is reverse-biased and the output voltage during this interval is equal to the capacitor voltage V_o.

In Figure 5 the circuit operation in MODE 2 is shown. Here S_1 is turned off and the output diode D_{o1} is forward biased. During this interval, the current through inductor L_1 falls linearly, as it discharges it's current to the load through i_{Cb1} and i_{Do1} and create the return path through diode D_{s2}. The inductor, L_2 will discharge its current linearly to the load through i_{Do1}. The current flowing through output diode D_{o1} is the summation of currents through inductors L_1 & L_2, i_{L1} and i_{L2} respectively. The peak current through diode D_{o1} is given by equation (2).

$$i_{do1pk} = d_1 T_s \left(\frac{V_g}{L_1} + \frac{V_{cb1}}{L_2}\right) \tag{2}$$

Since $V_{cb1} \approx V_g$, equation (2) becomes

$$i_{do1pk} = d_1 T_s \left(\frac{V_g}{L_a}\right) \tag{3}$$

Where $L_a = L_1//L_2$. The peak current flowing through switch S_1 is exactly the same with D_{o1} due to the summation of current at inductors L_1 and L_2. The d_2 width can be determined by examining the ripple current at inductor L_1 such that,

$$d_2 = \frac{V_g}{V_{cb1} + V_o - V_g} d_1 \tag{4}$$

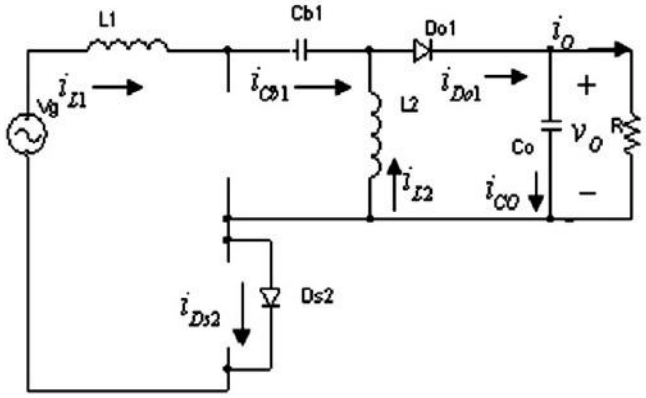


Figure 5. *Equivalent circuit during MODE 2 (d_2T_S)*

Finally, in MODE 3, both switch S_1 and diode D_{o1} are turned off as shown in Figure 6. During this interval energy at inductors L_1 and L_2 are equal and input voltage, Vg is equal to V_{Cb1}. As a result, almost zero current flows. However, an almost DC current exist and the current through inductors L_1 and L_2 are equal but on the opposite direction.

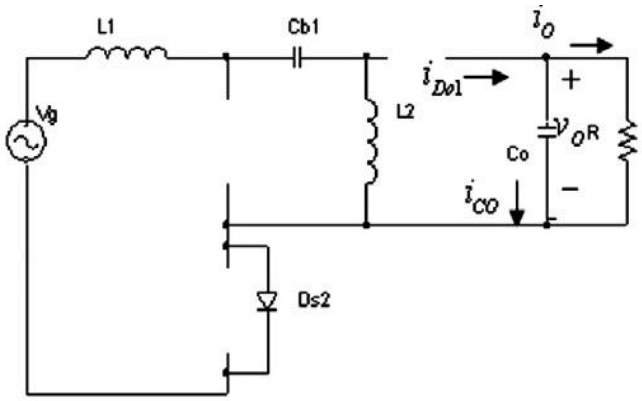


Figure 6. *Equivalent circuit during MODE 3 (d_3T_S)*

By equating the average current of D_{o1} with the output current, $i_o = V_o/R$, the relationship between input and output voltage is obtained. The voltage conversion ratio for the converter is given in equation (5),

$$M = \frac{\mathrm{Vo}}{Vg} = d_1\sqrt{\frac{RT_s}{2L_a}} \tag{5}$$

Where R is the resistive load value. To ensure discontinuous conduction mode operation for each switching period, the component selection must follow this equation,

$$1 - d_1 > \sqrt{\frac{2L_a}{RT_s}} \tag{6}$$

3. RESULTS AND DISCUSSIONS

A Bridgeless SEPIC PFC circuit is simulated for closed loop operation using MATLAB/SIMULINK. The design parameters used are given in Table I.

Table I. *Design Parameters*

Input Voltage, V_g	230V, 50Hz
Inductor, L_1	150µH
Inductors, L_2 & L_3	70µH
Capacitors, C_{b1} & C_{b2}	1µF
Output Capacitor, C_o	2200µF
Output Voltage, V_o	50V DC
Switching Frequency, f_s	50kHz
Rated Output Power	100W
Load Resistance	25Ω

In Figure 7 the closed loop SIMULINK Model of the circuit is shown. The simulation results for input voltage & input current and output voltage and output current are shown in Figure 8 & 9 respectively. Input current and input voltages are almost sinusoidal. The output voltage is a constant DC with value 50V.

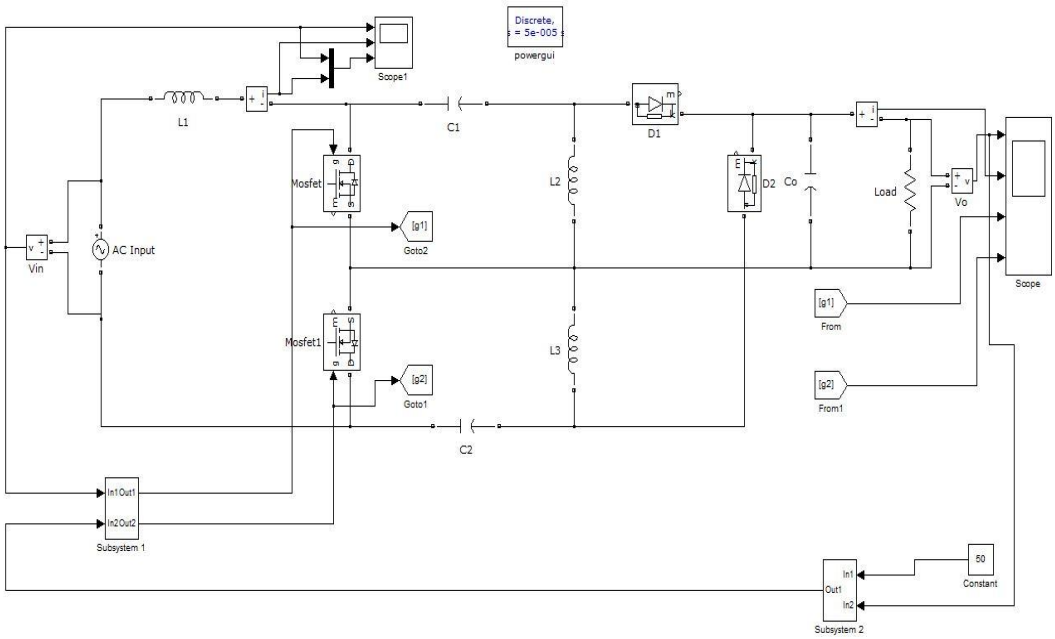


Figure 7. *Closed Loop SIMULINK Model of Bridgeless SEPIC PFC*

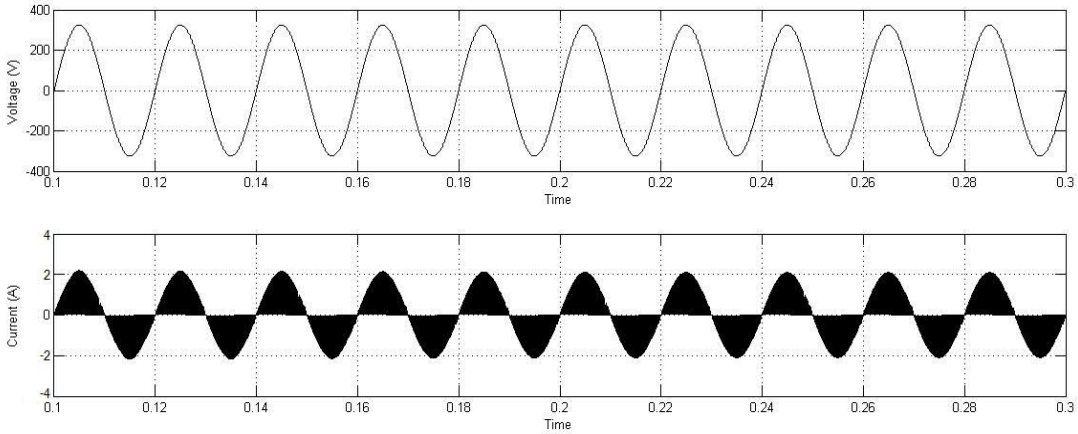


Figure 8. *Simulation results for input voltage & input current for closed loop operation*

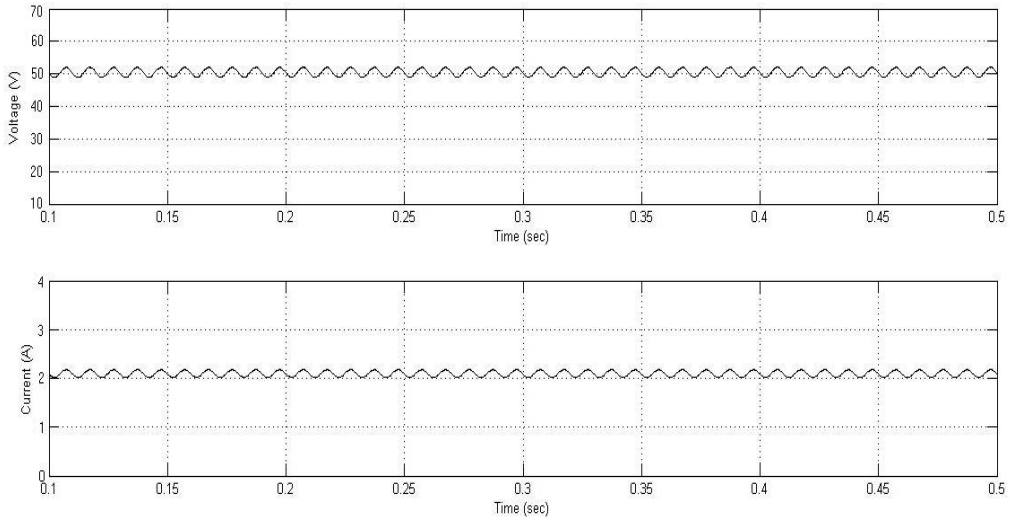


Figure 9. *Simulation results for output voltage and output current*

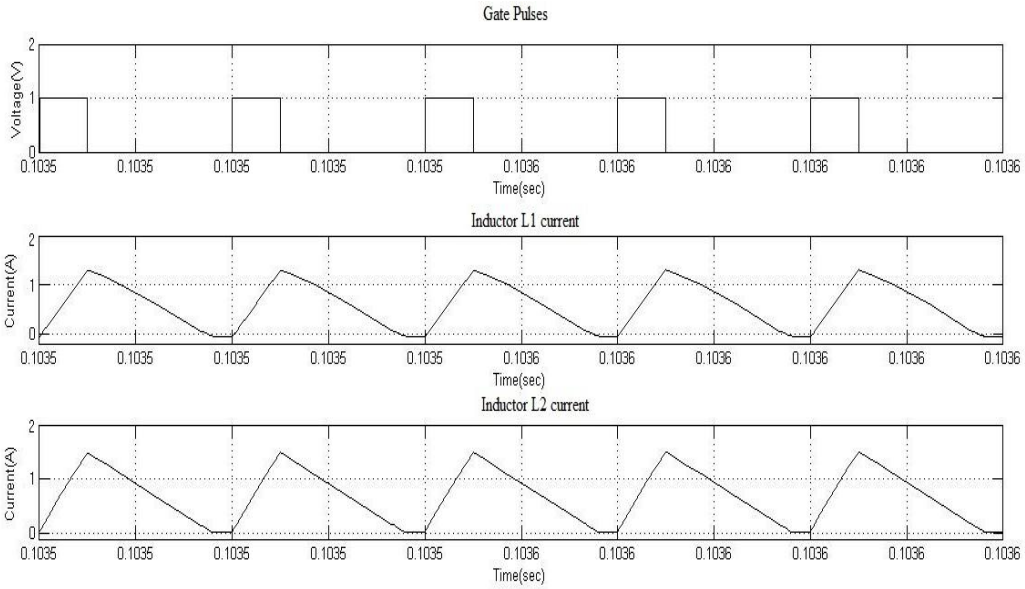


Figure 10. *Gate Pulses for Switch and Current through Inductors L_1 and L_2*

During positive half cycle of operation when switch S_1 is turned ON the current through both the inductors increases linearly, which corresponds to mode 1 operation. When the switch S_1 is turned OFF, the inductor current decreases linearly to zero from its peak value and corresponds to mode 2 operation. The region where the inductor current remains zero represents mode 3 operation.

In Figure 11 the current through diode Do1 is shown. During Mode 1 the diode does not conduct and in Mode 2 it is forward biased and conducts. In Mode 3 it remains OFF.

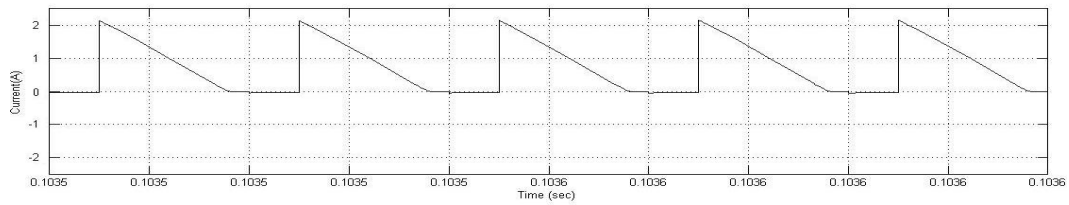


Figure 11. *Current through diode D_{o1}*

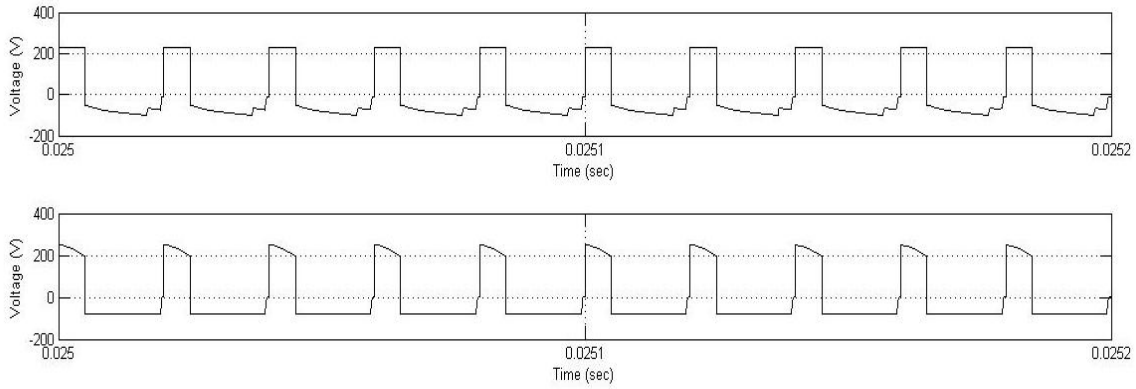


Figure 12. *Voltage across inductors L_1 and L_2*

The harmonic spectrum for closed loop operation is shown in Figure 13. THD is obtained as 11.42% and the power factor calculated is 0.9934. So the designed converter shapes the input current to be in phase with the input voltage and considerably reduces the THD.

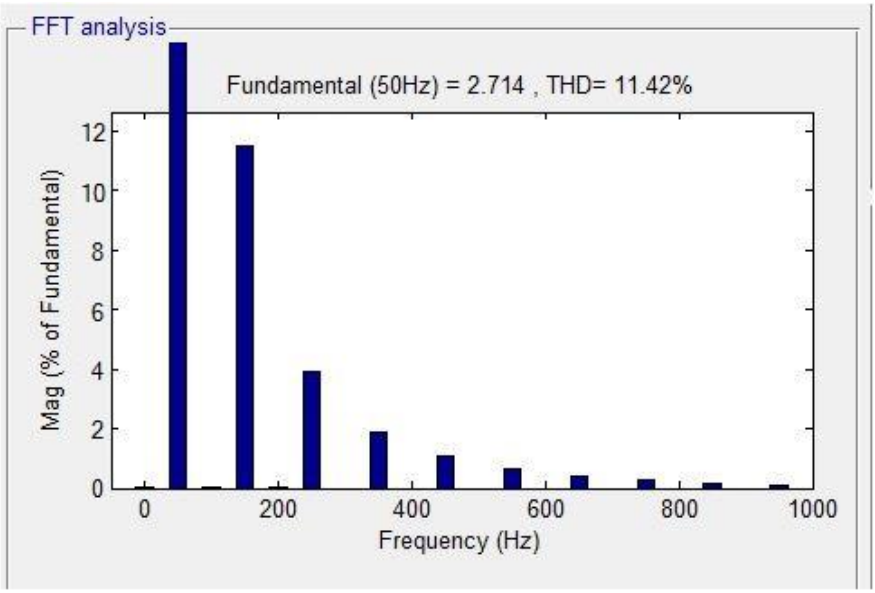


Figure 13. *Harmonic Spectrum for closed loop operation*

In Table II the power quality observation at different loads are shown. From the analysis it is noticed that the THD increases with the decrease in load. Also the power factor decreases slightly with the decrease in load.

Table II. *THD and Power Factor at different loads*

Load	THD (%)	Power Factor
100 W	11.42	0.9934
75 W	11.76	0.9931
50 W	12.31	0.9925
25 W	14.20	0.990

A prototype model of the Bridgeless SEPIC converter is designed and fabricated on a dot board. The control circuit for the converter is also designed. The input to the power circuit is 230V 50 Hz AC. The circuit was designed for 100W load. The hardware setup of the circuit is shown in Figure 14.

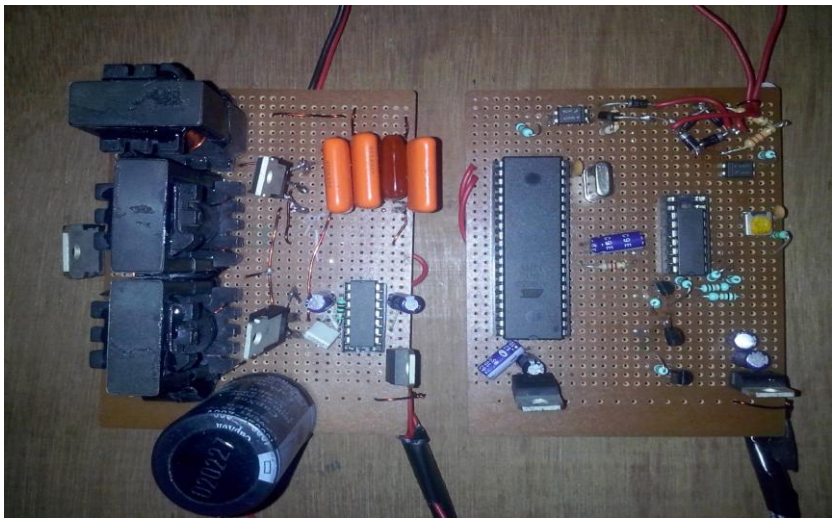


Figure 14. *Hardware setup of Bridgeless SEPIC PFC*

4. CONCLUSIONS

A bridgeless SEPIC Power Factor Correction circuit has been presented in which the input diode bridge rectifier is eliminated and thereby the number of conducting components is reduced. During each half cycle a maximum of eight components conduct. Thus the conduction losses are considerably reduced when compared to conventional PFC circuits. The circuit operation of the converter is discussed in detail and closed loop simulation of the circuit is done. From the simulation results, it is clear that the input voltage and input current are almost in phase and the power factor is high. This circuit would be most suitable to be used as a switch mode power supply application for low power equipments, especially those requiring high quality input power.

REFERENCES

[1] Nedmohan, Power Electronics Converters, Applications and Design, Third Edition, Wiley-India Edition, 2012.

[2] J. Wang, W. G. Dunford, and K. Mauch, "Analysis of a ripple-free input current boost converter with discontinuous conduction characteristics," IEEE Transactions on Power Electronics, vol. 12, no. 4, pp. 684–694, July 1997.

[3] Jian Sun, "On the Zero-Crossing Distortion in Single-Phase PFC Converters, IEEE Transactions on Power Electronics, vol. 19, no. 3,pp 685-692, May 2004.

[4] R. Martinez and P. N. Enjeti, "A high performance single phase rectifier with input power factor correction," IEEE Transactions on Power Electronics, vol. 11, no. 2, pp. 311–317, March 1996.

[5] M. Mahdavi and H. Farzanehfard, "Bridgeless SEPIC PFC rectifier with reduced components and conduction losses," IEEE Transactions on Industrial Electronics, vol. 58, no. 9, pp. 4153–4160, Sep. 2011.

[6] Esam H. Ismail, "Bridgeless SEPIC Rectifier with Unity Power Factor and Reduced Conduction Losses", IEEE Transactions on Industrial Electronics, vol. 56, no. 4, April 2009.

[7] Mohd Rodhi Sahid, Abdul Halim Mohd Yatim, "Modeling and simulation of a new Bridgeless SEPIC power factor correction circuit", IEEE Conference on Industrial Electronics, vol. 57, no. 6, pp 599-611, April 2011.

[8] Jae-Won Yang and Hyun-Lark Do, "Bridgeless SEPIC Converter with a Ripple-Free Input Current", IEEE Transactions on Power Electronics, vol. 28, no. 7, July 2013.

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