Design of Low Voltage Low Power Inverter Based Comparator Using CMOS Technology

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Abstract: *A new CMOS dynamic comparator uses dual input and dual output inverter based amplifier as latch stage, which is suitable for high speed analog-to-digital converters, low power dissipation and immune to noise as well as decreases delay than the previous work. Back to-back inverter in the latch stage is replaced with dual-input, dual output inverter based amplifier. This topology totally removes the noise, which is present in the input. The circuit is simulated with <2V DC supply voltage and 250 MHz clock frequency. The circuit has been designed by using 0.25 μm CMOS technology under 2V supply. This topology is based on two cross coupled differential pairs, has positive feedback and switchable current sources with less area, it is shown to be very robust against transistor mismatch. The simulation results will be shown by using tannerEDA software.*

Keywords: *CMOS comparator, low power, High Speed, Analog-to-Digital Converter and Tanner EDA*

1. INTRODUCTION

Comparators are mostly used in electronic components after operational amplifiers. Comparators are also known as 1-bit analog-to digital converter. So they are mostly used in large abundance in A/D converter. In the analog-to-digital conversion process, it is necessary to sample the input. This sampled signal is applied to comparators, to determine the digital equivalent of the analogsignal.In today's world, portable battery operator devices are increasing, because of low power methodologies are used for high speed applications. Power reduction can be achieved by moving towards smaller size processes. However, as we move towards smaller feature size, these process variations and other non-idealities will greatly affect the overall performance of the device. One such application where low power dissipation, low noise ,high speed, less hysteresis , less Offset voltage is required to Analog to Digital converters for mobile and portable devices. The accuracy of comparators are defined by its offset, along with power consumption, speed is of keen interest in achieving overall higher performance of ADCs. In the past, pre-amplifier based comparators are used for ADC architectures such as flash and pipeline. The main drawback of pre-amplifier based comparator is its offset voltage. To overcome this problem, dynamic comparators are often used to make a comparison once every clock period and require much less offset voltage. However, these dynamic comparators are suffered from large power dissipation compared to pre-amplifier based comparators. The main problem of these dynamic comparators is the output signal of latch stage is fluctuating during clock transition. This is happening due to the presence of noise at input terminals. The propose inverter based differential amplifier topology eliminates the noise at input side. It also reduces the delay and power consumption.

2. NEED OF THIS WORK

Traditional operational amplifier designs most commonly use transistors in the saturation region, which generally requires at least one DC bias current. As technology size has decreased, low power, high gain amplifier design has become more challenging for designers. Transistor threshold voltage generally doesn't decrease the feature size and power supply voltage, many cascaded or folded

designs are not possible with reduced voltage supply. Given that the reduction in headroom reduces the ability to cascade devices, low voltage high-gain amplifiers are commonly built by expanding outward, using two or even three cascaded amplification stages. These multi-stage cascaded designs require the designer to take extra measures to ensure amplifier stability, and, depending on the topology, it can be very challenging or complex to stabilize. Most stabilization schemes require additional compensation capacitors and/or nulling resistors, which use additional silicon area, and can decrease circuit bandwidth; however, these compensation reduced power supply voltage and the increasing demand for low power consumption make sub-threshold operation and design a more viable alternative when a reduction in bandwidth is acceptable. Operation in the sub-threshold region causes the drain current to increases exponentially with VGS as opposed to quadratically in the saturation region. The disadvantage with sub-threshold operation is the reduction in amplifier driving current, and the loss of ability to quickly drive large capacitive loads.

In this work, an inverter-based operational amplifier topology and operation and design principles are discussed and evaluated. We use two previously used figures of merit to objectively compare various aspects of the different circuit topologies. We conclude that the inverter-based differential amplifier topology with current starving provides one of best circuit topologies for energy efficiency.

3. DESIGN PROCESS OF EXISTING WORK

Figure.1shows the schematic diagram of the double tail comparator. Double tail architecture has additional two tail connections. During the RESET PHASE, when Clk is LOW (Clk =0), transistor NMOS_5 and PMOS_3 are inoff state and PMOS_6, PMOS_7, are in on state. Transistors PMOS_4 and PMOS_5 are in cut-off mode. Switch transistors PMOS_3, PMOS_6, PMOS_4, and PMOS_7 will charge the drains of transistors NMOS_ 1 and NMOS_2 and the output nodes Outp and Outn towards Vdd. During the REGENERATION PHASE, when Clk is HIGH (Clk =1),The process starts by turning the transistor NMOS_3 on and immediately an current 'I' starts to flow and the drain of transistor NMOS_3 starts to discharge towards ground (Gnd).In this succession the differential input transistors NMOS_3 and NMOS_4 are turned on. Current of transistors NMOS_1 and NMOS_2, (at the drain terminal) will start to pull the output nodes Outp and Outn towards Gnd. Due to the voltage differences between the input signals, the current at the drain terminals of transistors NMOS_ 3 and NMOS_4 will be different. In the regeneration mode the output node is discharging towards Gnd and pmos transistors PMOS_1 and PMOS_2 will come into saturation region. This design is simulated by using 0.25μm CMOS Technology using Tanner EDA Tools.
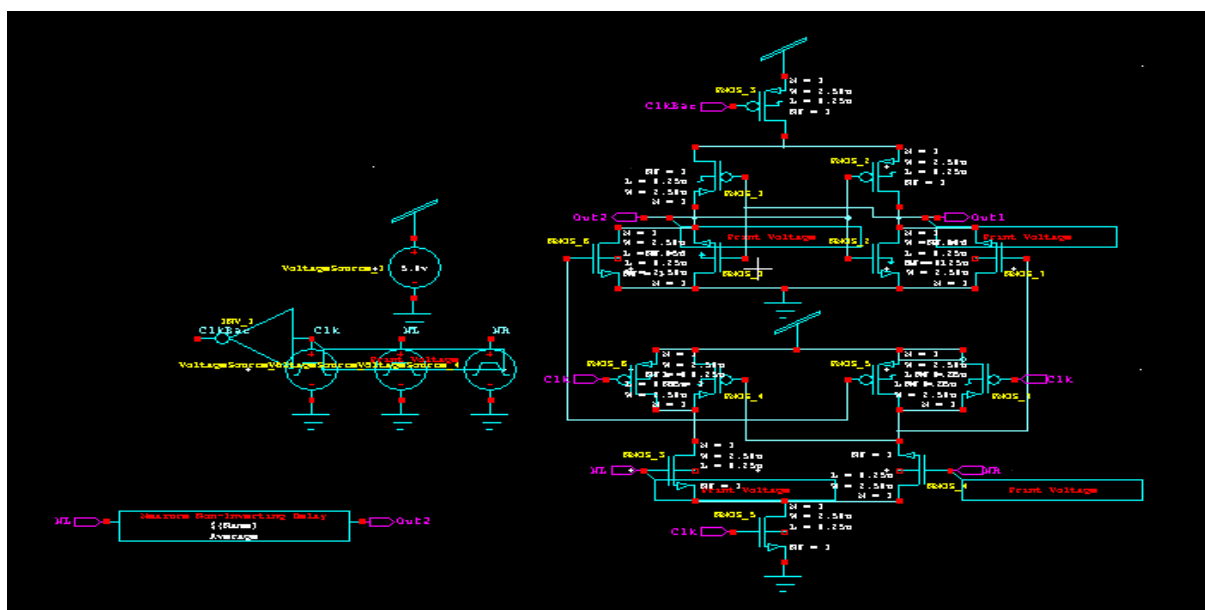
Existing Dynamic Comparator

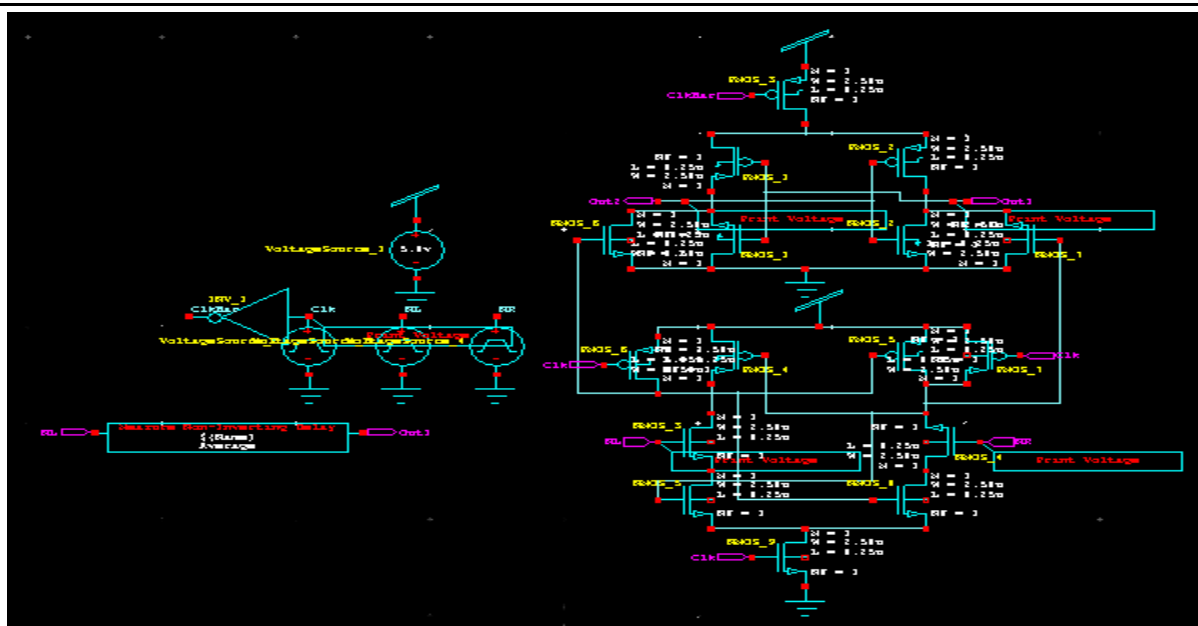**Figure 1.** *Main Idea of dynamic comparator*

Figure 2. *Final structure of dynamic comparator*

Figure 2 shows the final structure ofdouble tail comparator.For its operation, during the pre-charge (or reset) phase (Clk=0V), both PMOS transistor PMOS_6 and PMOS_7 are turned on and they charge Di nodes' capacitance to VDD, which turn both NMOS transistor NMOS_1 and NMOS_2 of the inverter pair on and Di' nodes discharge to ground. Sequentially, PMOS transistor PMOS_1, PMOS_2, PMOS_6 and PMOS_7 are turned on and they make out nodes and SW nodes to be charged to VDD while both NMOS transistors NMOS_4 and NMOS_3 are being off. During the evaluation phase (Clk=VDD), each Di node capacitance is discharged from VDD to ground in a different time rate proportionally to the magnitude of each input voltage. Input voltage is formed between Di+ and Di- node. Once either Di+ or Di- node voltage drops down below around VDD−|Vtp|, the additional inverter pairs PMOS_1/ NMOS_1and PMOS_2/ NMOS_2 invert each Di node signal into the regenerated Di' node signal. Then the regenerated and different phased Di' node voltages are amplified again and relayed to the output-latch. The additional Feedback transistors NMOS_5 and NMOS_8 which used for reducing the static loss effect which was suffered by the before comparator design.due to this, comparator has less stacking and it has only one current path via tail transistor.

4. DESIGN PROCESS OF PROPOSED WORK

Sub Threshold

Sub threshold leakage or sub threshold drain current is the current between the source and drain of a MOSFET when the transistor is in sub threshold region or in weak-inversion region, that means gate-to-source voltages below the threshold voltage. But in the sub threshold conduction of transistors has usually been very small in the *off* state, as gate voltage could be significantly below the threshold, but as voltages have been scaled down with transistor size, subthreshold conduction has become a bigger factor.

The reason for a growing importance of subthreshold conduction is that the supply voltage has continually scaled down, both to reduce the dynamic power consumption of integrated circuits, and to keep electric fields inside small devices low, to maintain device reliability. The amount of sub threshold conduction is set by the threshold voltage, which sits between ground and the supply voltage that has to be reduced along with the supply voltage. That reduction means, it has less gate voltage swing below the threshold to turn *off* the devices, and as subthreshold conduction varies exponentially with gate voltage.

To reduce the sub threshold effect here we uses the stacking scheme an design of inverter based amplifier was proposed
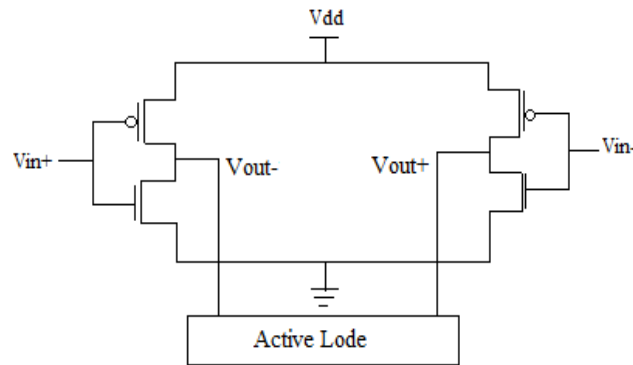
Figure 3. *Inverter Based amplifier Design*

The inverter-based amplifier topology shown in Figure 3 uses CMOS inverters as the amplifier input. This input stage design has the advantage of combining the transconductance of the n and p transistors. This combination of the two transconductances should provide increase in gain over a traditional common source amplification stage, with approximately the same DC bias current. When this architecture is implemented with a standard supply voltage (>2vt), the overall transconductance can be increased significantly depending on how transistors in the inverters are sized and the resulting current through the inverter. High current through the inverter allows significantly high bandwidths to be achieved. Another advantage of this topology is an increase in output swing and linearity when compared to a traditional common source or cascade amplifier if the respective transconductances of the p and n type transistors are approximately equal in magnitude. For noise, the inverter-based topology offers lower equivalent noise resistance compared to the equivalent common source topology.
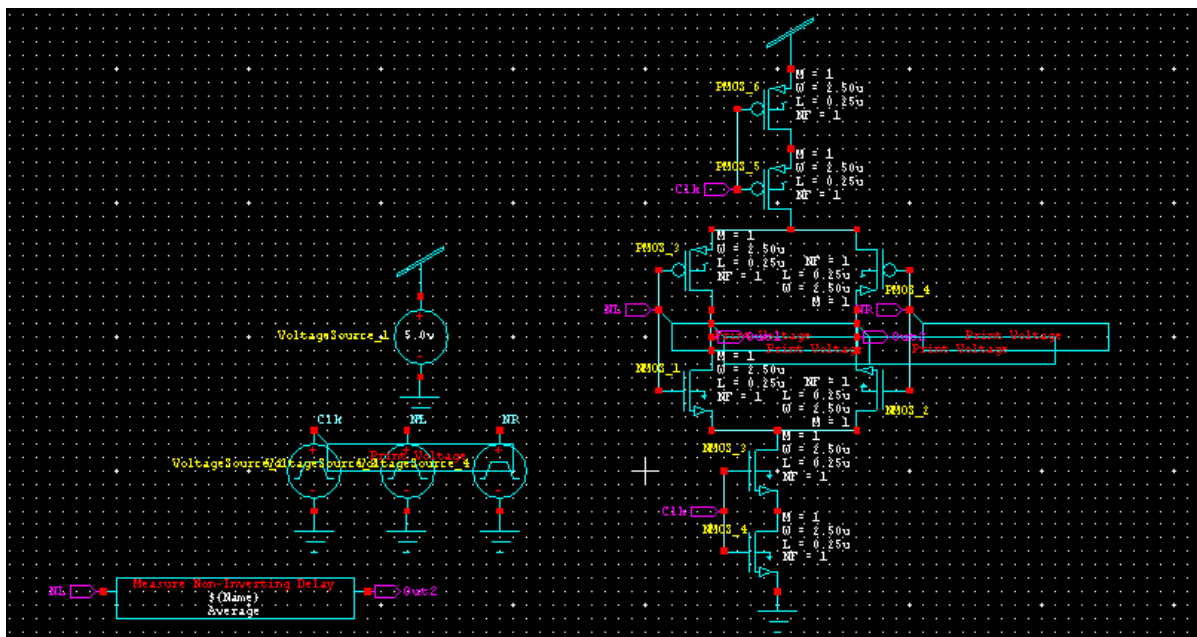

Figure 4. *Inverter based amplifier design with reduced Subthreshold*

Figure 4 shows the Inverter based amplifier design with reduced Subthreshold. In this design two additional transistors are connected in series at pull up &pull down side to increases the resistance of the circuit. HerePMOS_5, PMOS_6 and NMOS_3 and NMOS_4 constitute the stacking scheme for the comparator which reduces the sub-threshold effect of a comparator by providing high resistance in the off region. During reset phase (CLK=0), both pmos transistors PMOS-5, PMOS-6 will be in on state&nmos transistors NMOS-3, NMOS-4 will be in off state. Then both outputs will be in high. During decision making phase (CLK=VDD), both pmos transistors are in off state and nmos transistors are turned on .the currents of nmos-3, nmos-4 will start to pull the output nodes out1 and out2 towards gnd.
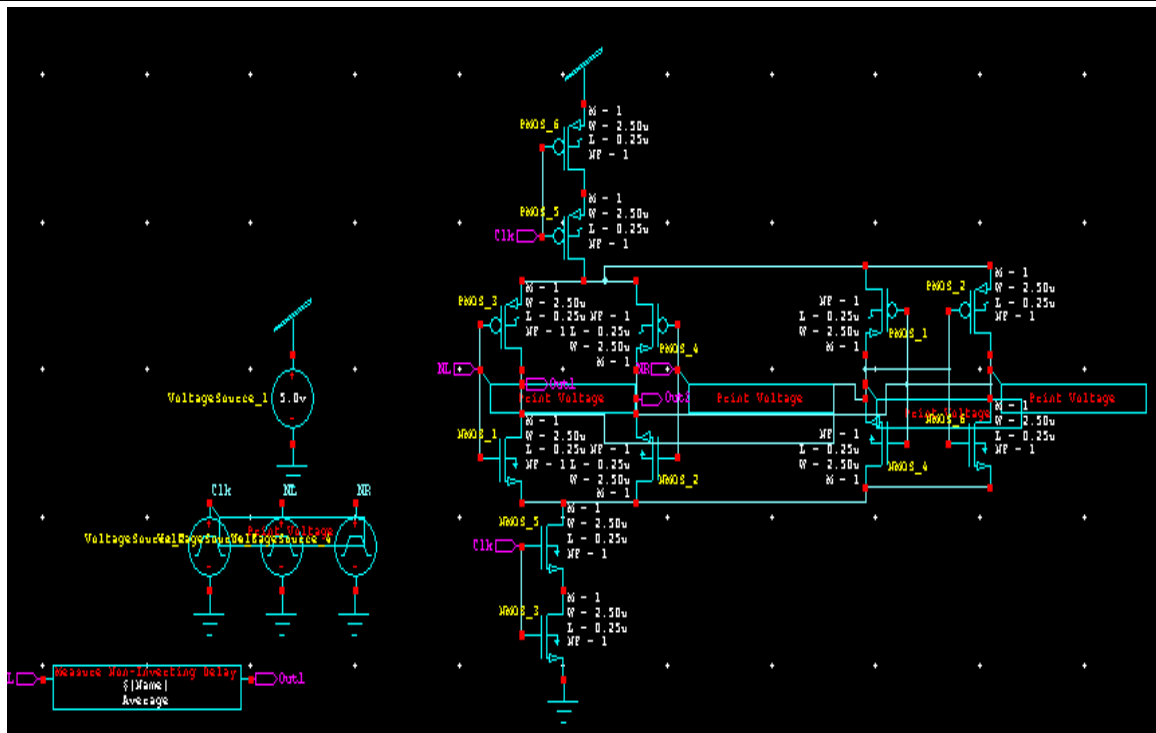
Figure 5. *Inverter Based Amplifier with Latch network across*

Figure 5 demonstrates the schematic diagram of Inverter Based Amplifier with Latch network across subthreshold circuit. TransistorsPMOS_3 / NMOS_1 and PMOS_4/NMOS_2 are the inverter pairs through which differential inputs are fed across the outputs of the latch network. which was connected by PMOS_1/NMOS_4 and PMOS_2 / NMOS_6 are acts like latch network which will increases the gain factor and decreases the delay of the comparator The cross coupled pair provides positive feedback and therefore a negative resistance of -2/gm3.it will gives the output without any noise. In this circuit the output of subthreshold network is given to the input for latch network .it will totally removes the noise and gives complete logic high voltage at one output side. Proposed design will be reduced delay and increases speed with a 5.0 V supply. This design is simulated by using 0.25µm CMOS Technology using Tanner EDA Tools. This design can be used where high speed and low propagation delay are the main parameters schemes have been improving with the usage of active compensation networks.

5. RESULTS

These Circuits are Simulated Using Tanner Tools
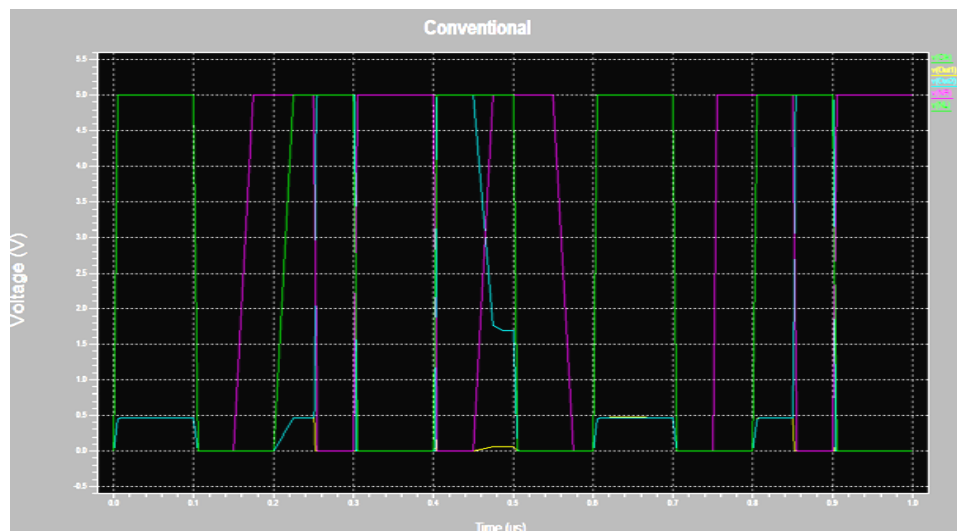
The results are compared with the existing Technique.

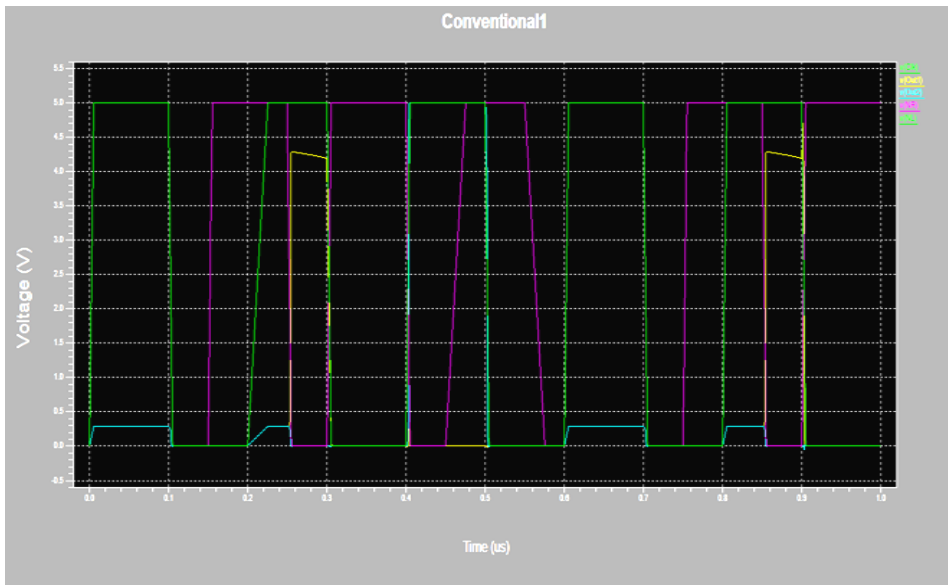**Figure 6.** *Simulation result for main idea of dynamic comparator*

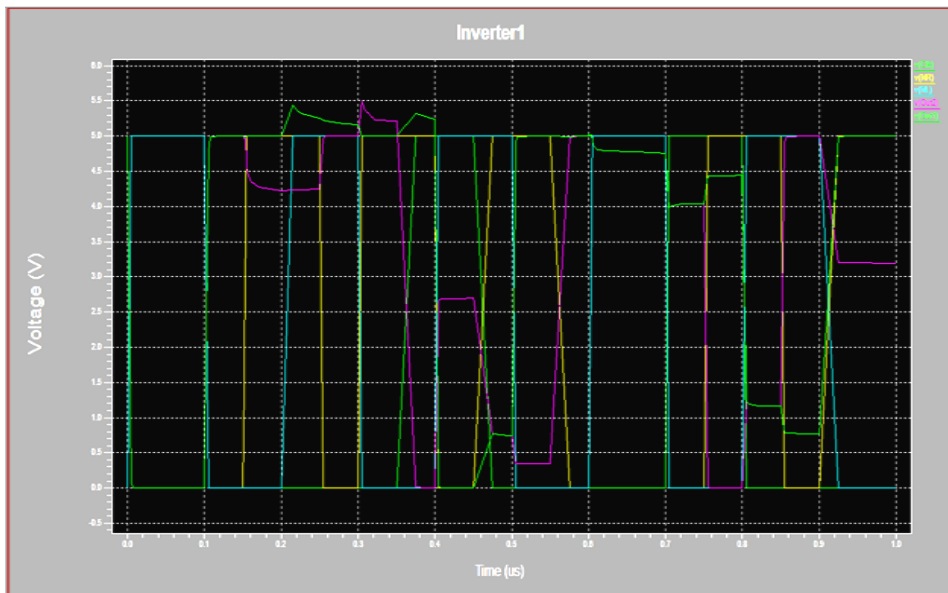**Figure 7.** *Simulation result for final structure of dynamic comparator*

Figure 8. *Simulation result of Inverter based amplifier design with reduced Sub threshold*
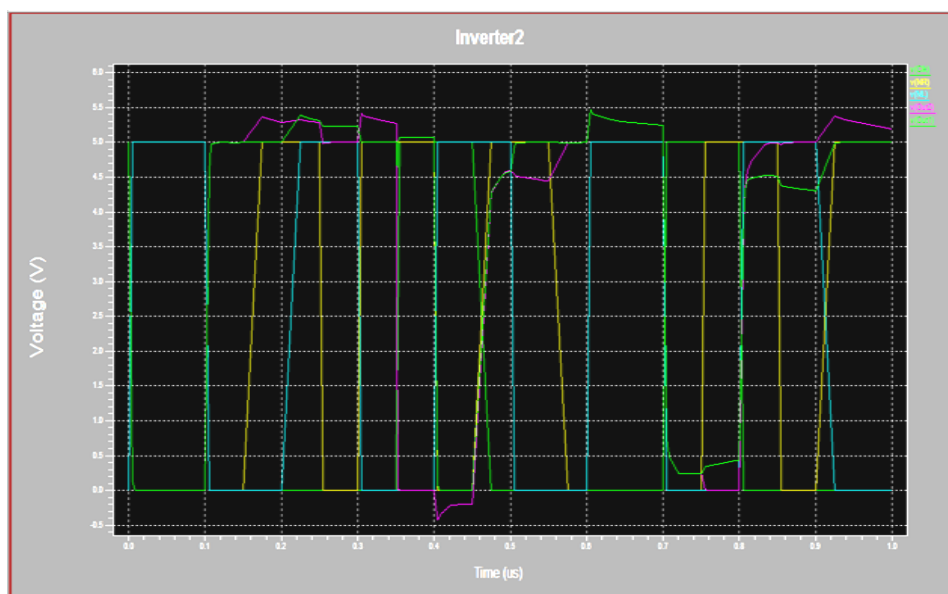

Figure 9. *Simulation result of Inverter Based Amplifier with Latch network across*

The tabulation of performance comparison of existing and proposed methods is shown below. The active device has considerably increased when compared to the proposed methods. The area of the proposed works has got comparatively increased with the existing methods.

Circuit	Delay	Power Dissipation
Main idea of dynamic comparator	$2.2489*10^{-7}$sec	$1.777379*10^{-5}$W
Final Structure dynamic comparator	$2.2555*10^{-7}$Sec	$5.148283*10^{-6}$W
Inverter Based amplifier design with reduced subthreshold	$6.9984*10^{-11}$Sec	$1.501981*10^{-6}$ w
Inverter Based amplifier with latch network	$1.4823*10^{-10}$ Sec	$2.777180*10^{-9}$w

6. CONCLUSION

In this project the Inverter-based amplifier design with reduced subthreshold and latch network across feature has been evaluated. latched network was designed that works with high speed and low power consumption when compared to double tail latched comparator and pre amplifier based clocked comparator.While the idea of inverter based amplifiers is not conceptually novel, the idea of better controlling the current through the inverters using the concept of subthreshold and latch network for low power applications, as well as decreases the delay time and common-mode control makes the concept of inverter-based amplifiers more practical in real applications, particularly for applications for low power and low supply voltages. The simulation results show that the proposed circuit can operate at higher speed with low power dissipation as well as decreases the delay time also.

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