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SIC Vector Generation Using Test per Clock and Test per Scan

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Abstract: *Digital circuit complexity increasing day to day at the same time, more quality and reliability are necessary. In this paper we proposed a Test pattern generation for BIST. Actually in baSIC LFSR power consumption is high, i.e., all flip flops active even single bit change then power is high. To overcome we can use low power linear feedback shift register this is existing method. This paper is proposed method to existing low power Linear Feedback Shift Register. This paper explains the Automatic test pattern generation on Built in Self Test. Our method gives a solution for this. In this project only SIC (one input change). And we can generate a Different One input change stages. In this each vector applied to a scan chain is an SIC vector. A Johnson counter and scalable SIC counter are developed to generate minimum transition. And one more advantage is this is flexible to both Test-per-clock and Test-per-scan schemes. Different One input change save the test power imposes no more than 7.5% overhead. It increases the fault coverage without increasing the length.*

Keywords: *Bist,Lfsr,Lp-Lfsr,One Input Change*

1. Introduction

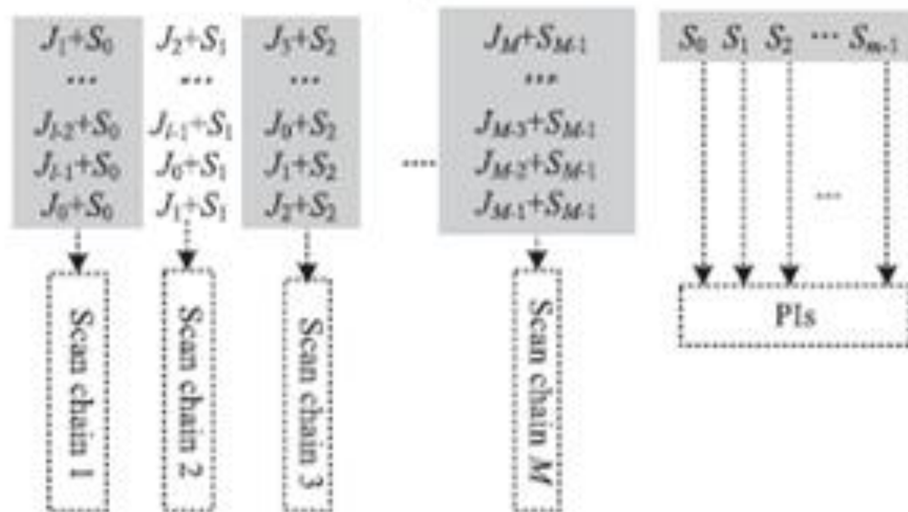
BUILT-IN SELF-TEST (BIST) techniques can effectively reduce the difficulty and complexity of VLSI testing, by introducing on-chip test hardware into the circuit-under-test (CUT). In conventional BIST architectures, the linear feedback shift register (LFSR) is commonly used in the test pattern generators (TPGs) and output response analyzers. A major drawback of these architectures is that the pseudorandom patterns generated by the LFSR lead to significantly high switching activities in the CUT [1], which can cause excessive power dissipation. They can also damage the circuit and reduce product yield and lifetime [2]. In addition, the LFSR usually needs to generate very long pseudorandom sequences in order to achieve the target fault coverage in nanometer technology. Several advanced BIST techniques have been studied and applied. The first class is the LFSR tuning. Girard *et al.* analyzed the impact of an LFSR's polynomial and seed selection on the CUT's switching activity, and proposed a method to select the LFSR seed for energy reduction [4].

The second class is low-power TPGs. One approach is to design low-transition TPGs. Wang and Gupta used two LFSRs of different speeds to control those inputs that have elevated transition densities [5]. Corno *et al.* provided a lowpower TPG based on the cellular automata to reduce the test power in combinational circuits. Another approach focuses on modifying LFSRs. The scheme in reduces the power in the CUT in general and clock tree in particular. In , a low-power BIST for data path architecture is proposed, which is circuit dependent. However, this dependency implies that nondetecting subsequences must be determined for each circuit test sequence. Bonhomme *et al.* used a clock gating technique where two nonoverlapping clocks control the odd and even scan cells of the scan chain so that the shift power dissipation is reduced by a factor of two. The ring generator can generate a single-input change (SIC) sequence which can effectively reduce test power. The third approach aims to reduce the dynamic power dissipation during scan shift through gating of the outputs of a portion of the scan cells. Bhunia *et al.* inserted blocking logic into the stimulus path of the scan flip-flops to prevent the propagation of the scan ripple effect to logic gates. The need for transistors insertion, however, makes it difficult to use with standard cell libraries that do not have power-gated cells. In the efficient selection of the most suitable subset of scan cells for gating along with their gating values is studied.

2. Proposed Multiple Single Input Change

This section develops a TPG scheme that can convert an SIC vector to unique low transition vectors for multiple scan chains. First, the SIC vector is decompressed to its multiple codewords[3]. Meanwhile, the generated codewords will bit-XOR with a same seed vector in turn. Hence, a test

pattern with similar test vectors will be applied to all scan chains. The proposed MSIC-TPG consists of an SIC generator, a seed generator, an XOR gate network, and a clock and control block. Meanwhile, the generated code words will bit-XOR with a same seed vector in turn.



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2.1. TPG Method

There are m primary inputs (PIs)[9] and M scan chains in a full scan design, and each scan chain has scan cells. Fig. 1(a) shows the symbolic simulation for one generated pattern. The vector generated by an m-bit LFSR with the primitive polynomial can be expressed as the eqn is the S(t) = S0(t)S1(t)S2(t), . . . , Sm−1(t) (hereinafter referred to as the seed), and the vector generated by an l-bit Johnson counter can be expressed as J (t) = J0(t)J1(t)J2(t), . . .Jl−1(t).The first clock cycle, $J = J0\ J1\ J2, . .\ Jl-1$ will bit-XOR with $S = S0S1S2, . . . , SM-1$, and the results $X1Xl+1X2l+1, . . . , X(M-1)l+1$ will be shifted into M scan chains, respectively. In the second clock cycle, $J = J0J1\ J2, . . . , Jl-1$ will be circularly shifted as $J = Jl-1\ J0\ J1, . . . , Jl-2$, which will also bit-XOR with the seed eqn $S= S0S1S2, . . , SM-1$. The resulting $X2Xl+2X2l+2, ., . . X(M-1)l+2$ will be shifted into M scan chains respectively. After l clocks, each scan chain will be fully loaded with a unique Johnson codeword, and seed $S0S1S2, . . . , Sm-1$ will be applied to m PIs. Therefore circular Johnson counter can generate l unique Johnson code words through circular shifting a Johnson vector, the circular Johnson counter and XOR gates in Fig. 1 actually constitute a linear sequential de compressor.

2.2. Reconfigurable Johnson Counter

The different scenarios of scan length, this paper develop two kinds of SIC [6] generators to generate Johnson vectors and Johnson code words, i.e., the reconfigurable Johnson counter and the scalable SIC counter.

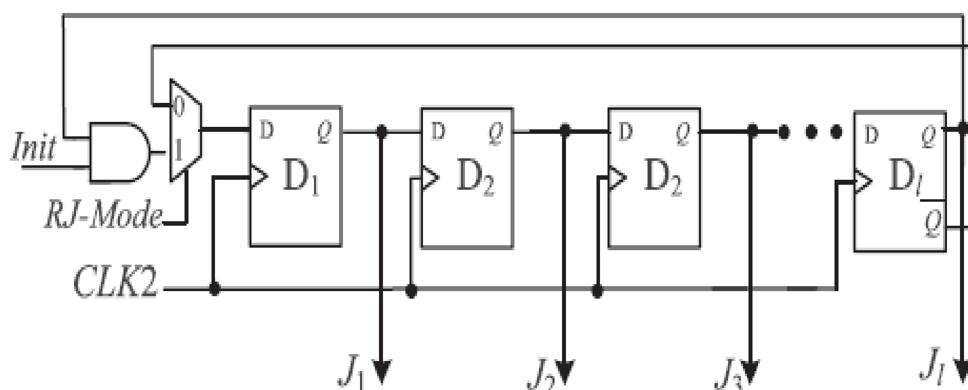

Fig2. *Reconfigurable Johnson counter*

For a short scan length, we develop a reconfigurable Johnson counter to generate an SIC sequence in time domain. As shown in Fig. 2. It can operate in three modes.

1) *Initialization:* When RJ_Mode is set to 1 and *In it* is set to logic 0, the reconfigurable Johnson counter will be initialized to all zero states by clocking CLK2 more than l times.

2) *Circular shift register mode:* When RJ_Mode and In it are set to logic 1, each stage of the Johnson counter will output a Johnson codeword by clocking CLK2 l times.

3) *Normal mode:* When RJ_Mode is set to logic 0, the reconfigurable Johnson counter will generate $2l$ unique SIC vectors by clocking CLK2 $2l$ times.

3. MULTIPLE SINGLE INPUT CHANGE SEQUENCE

The proposed algorithm is to reduce the switching activity. In order to reduce the hardware overhead, the linear relations are selected with consecutive vectors or within a pattern, which can generate a sequence with a sequential de compressor, facilitating hardware implementation. Another requirement is that the MSIC sequence should not contain any repeated test patterns, because repeated patterns could prolong the test time and reduce test efficiency.

3.1. Multiple One Input Change -TPGs for Test-Per-Clock Schemes

The MSIC-TPG for test-per-clock schemes is illustrated in Fig. 3. The CUT's PIs $X1 - Xmn$ are arranged as an $n \times m$ SRAM-like grid structure. Each grid has a two-input XOR gate whose inputs are tapped from a seed output and an output of the Johnson counter. The outputs of the XOR gates are applied to the CUT[7]'s PIs. A seed generator is an m-stage conventional LFSR, and operates at low frequency CLK1. The test procedure is as follows.

- The seed generator generates a new seed by clocking CLK1 one time.
- The Johnson counter generates a new vector by clocking CLK2 one time.
- Repeat 2 until $2l$ Johnson vectors are generated.
- Repeat 1–3 until the expected fault coverage or test length is achieved

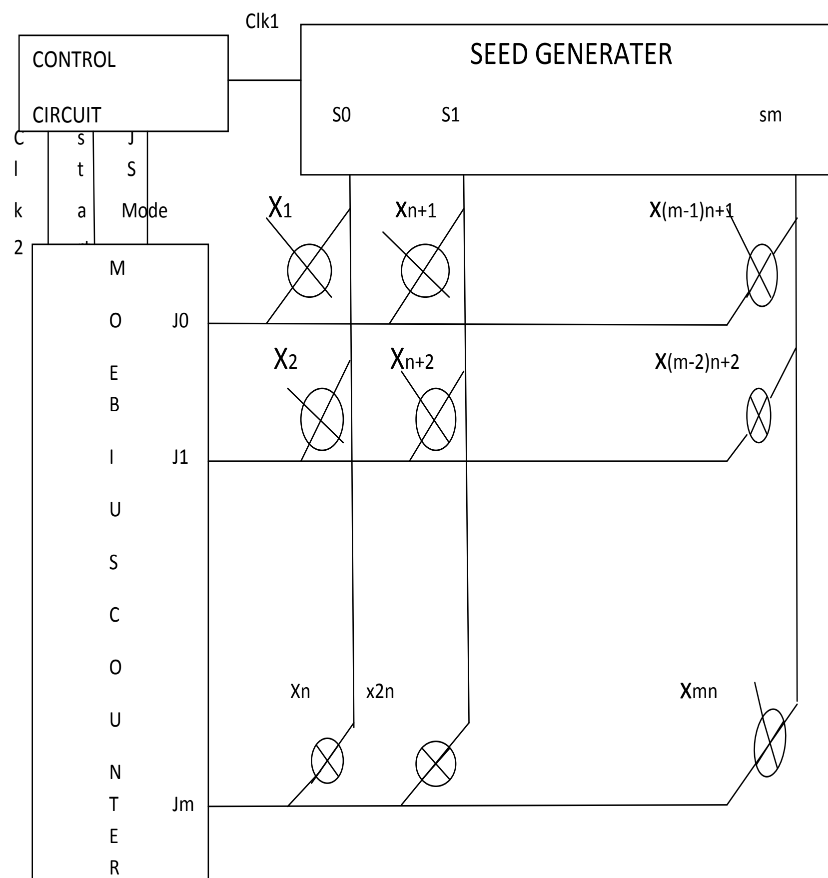

Fig3. *Test per clock with SIC*

3.2. MSIC-TPGs for Test-Per-Scan Schemes

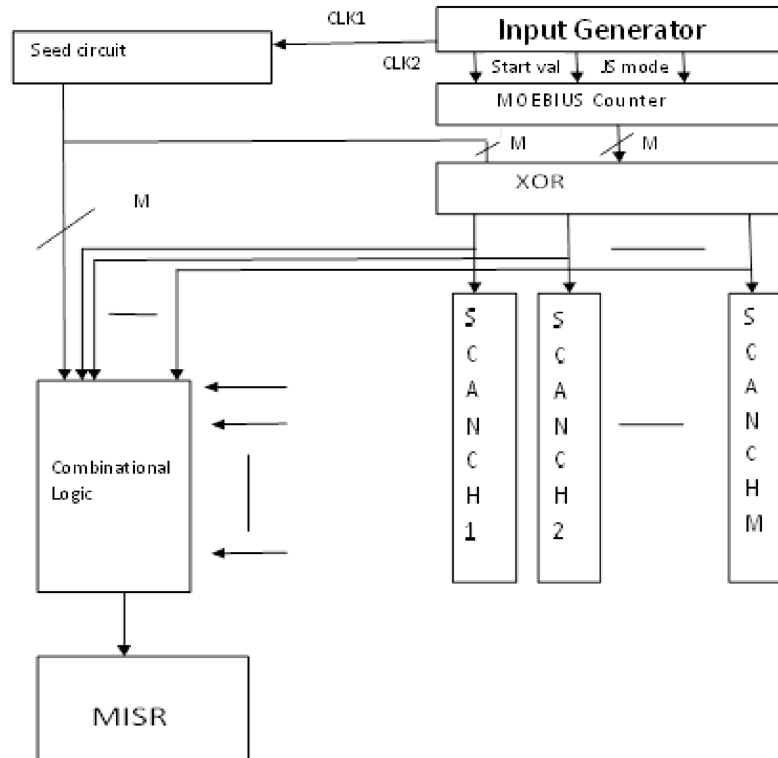

Fig4. *Test Per Scan with SIC*

The fig (4) shows inputs of the XOR gates come from the seed generator and the SIC counter, and their outputs are applied to *M* scan chains, respectively. The outputs of the seed generator and XOR gates are applied to the CUT's PIs, respectively. The test procedure is as follows.

- The seed circuit generates a new seed by clocking CLK1 one time.
- RJ_Mode is set to "0". The reconfigurable Johnson counter will operate in the Johnson counter mode and generate a Johnson vector by clocking CLK2 one time.
- After a new Johnson vector is generated, RJ_Mode and Init are set to 1. The reconfigurable Johnson counter operates as a circular shift register, and generates l code words by clocking CLK2 l times. Then, a capture operation is inserted.
- Repeat 2–3 until $2l$ Johnson vectors are generated.
- Repeat 1–4 until the expected fault coverage or test length is achieved.

4. Principle of MSIC Sequences

The main objective of the proposed algorithm is to reduce the switching activity. In order to reduce the hardware overhead, the linear relations are selected with consecutive vectors or within a pattern, which can generate a sequence with a sequential decompresor, facilitating hardware implementation. Another requirement is that the MSIC sequence should not contain any repeated test patterns, because repeated patterns could prolong the test time and reduce test efficiency [5].

Finally, uniformly distributed patterns are desired to reduce the test length (number of patterns required to achieve a target fault coverage). This section aims to extract a class of test sequences that meets these requirements.

5. Conclusion

The power reduction in TPS is less than the TPC. The pattern is using same things in both TPC and TPS but the stored in one scan chains is less power consuming. BIST controller is designed to monitor fault detection activity with logic and a signature generation element. The hold logic is operable to suspend signature generation in the signature generation element at any desired point in the test sequence. Signature mismatch with the reference signature means that the circuit is faulty

6. RESULTS

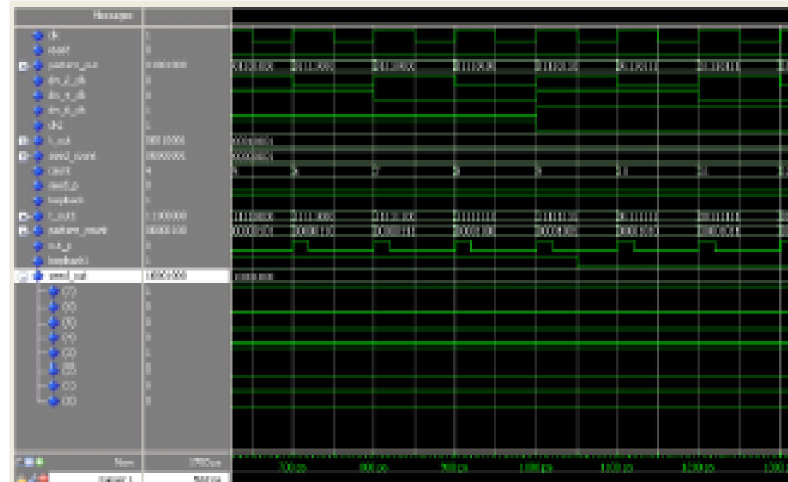

Fig6(a). *Test per Clock*

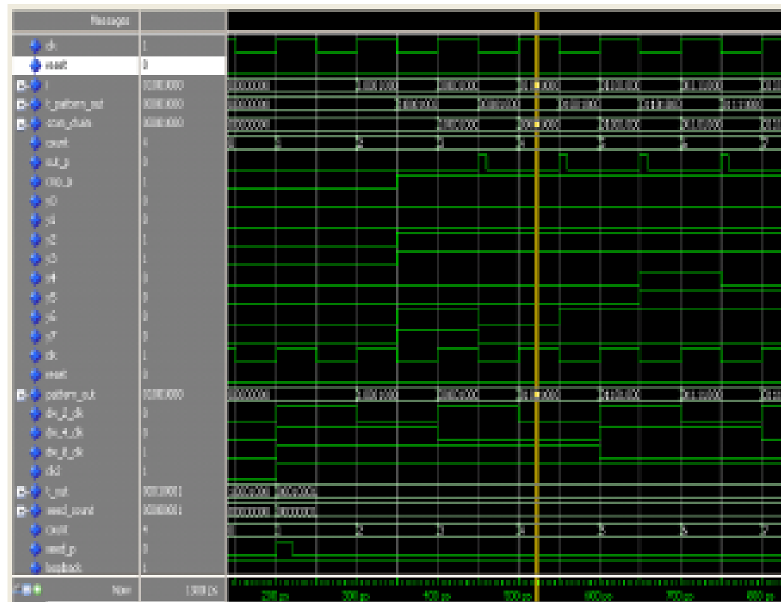

Fig6(b). *Test per scan*

REFERENCES

[1] P. Girard, “Survey of low-power testing of VLSI circuits,” *IEEE Design Test Comput.*, vol. 19, no. 3, pp. 80–90, May–Jun. 2002.

[2] A. Abu-Issa and S. Quigley, “Bit-swapping LFSR and scan-chain ordering: A novel technique for peak- and average-power reduction in scan-based BIST,” *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 28, no. 5, pp. 755–759, May 2009.

[3] S. Wang and S. Gupta, “DS-LFSR: A BIST TPG for low switching activity,” *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 21, no. 7, pp. 842–851, Jul. 2002.

[4] F. Corno,M. Rebaudengo, M.Reorda,G.Squillero, and M.Violante,”Low power BIST via non linear hybrid cellular automata,”in proc.18th IEEE VLSI Test symp., Apr-May 2000, pp 29-34.

[5] D. Gizopoulos, N. Krantitis, A. Paschalis, M. Psarakis, and Y. Zorian, “Low power/energy BIST scheme for datapaths,” in *Proc. 18th IEEE VLSI Test Symp.*, Apr.–May 2000, pp. 23–28.

[6] Y. Bonhomme, P. Girard, L. Guiller, C. Landrault, and S. Pravossoudovitch, “A gated clock scheme for low power scan testing of logic ICs or embedded cores,” in *Proc. 10th Asian Test Symp.*, Nov. 2001, pp. 253–258.

[7] C. Laoudias and D. Nikolos, “A new test pattern generator for high defect coverage in a BIST environment,” in *Proc. 14th ACM Great Lakes Symp. VLSI*, Apr. 2004, pp. 417–420.

[8] S.Bhunia, H. Mahmoodi, D. Ghosh, S. Mukhopadhyay, and K. Roy,

[9] “Low-power scan design using first-level supply gating,” *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 13, no. 3, pp. 384–395, Mar. 2005.

[10] X. Kavousianos, D. Bakalis, and D. Nikolos, “Efficient partial scan cell gating for low-power scan-based testing,” *ACM Trans. Design Autom. Electron. Syst.*, vol. 14, no. 2, pp. 28-1–28-15, Mar. 2009.