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Design and Performance Analysis of Low Power 6T SRAM Using Tanner Tool

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ABSTRACT

Memories are integral parts of most of the digital devices and hence reducing power consumption of memory is very important in improving the system performance, efficiency and stability. The requirement in present scenario is low power devices. Since these are critical component in high performanceprocessors. Keeping this point in view, this paper proposes on 6T CMOS SRAM. The Proposed and conventional 16-bit SRAM has been designed and simulated for 180nm, 100nm and 90nm CMOS technologies. The 16-bit memory is organized in 4 x 4 forms (i.e. 4 rows and 4 columns). The whole circuit verification is done on the Tanner tool, Schematic of the SRAM cell is designed on the S-Edit and net list simulation done by using T-spice and waveforms are analyzed through the W-edit. An asymmetric configuration has been implemented to reduce this leakage power. 6T SRAM cell is the best asymmetric configuration used as caches.

Keywords: CMOS logic, SRAM, VLSI, Read-Static Noise Margin (SNM), Stability and Power Consumption.

INTRODUCTION

According to International Technology Road Map for Semiconductors (ITRS), memory is expected to occupy about 90% of the chip area in 2013[1]. The reason is that everyone wants hand held electronic devices such as mobile phone, handy cam, tablets etc. to be as small as possible. At the same time, they should perform optimally in terms of performance, speed, battery life and a lot of storage space. Over the last few decades, scaling of conventional CMOS technology has been created two main problems; reliability and power consumption. This is possible only because of the technological advancement of low power high speed devices. Though, the contemporary high-speed devices use Static Random Access Memory (SRAM), for example in cache [2]. To achieve these objectives, the feature size of CMOS devices has been dramatically scaled to smaller dimensions.

Hence, power consumption of SRAM modules must be reduced and has been under extensive investigation in the technical literature. The goal of this paper is to design and comparative performance analysis of 16-bit SRAM 4 x 4 forms (i.e. 4 rows and 4 columns) at different technologies.

Static random access memory (SRAM) is a type of volatile semiconductor memory to store binary logic '1' and '0' bits. SRAM uses bi-stable latching circuitry made of Transistors MOSFETS to store each bit. When the cell is selected, the value to be written is stored in the cross-coupled flip-flops. A basic SRAM cell consists of two cross coupled inverters forming a simple latch as storage elements and two switches connecting these two inverters to complementary bit lines to communicate with the outside of the cell shown in fig-1[3].

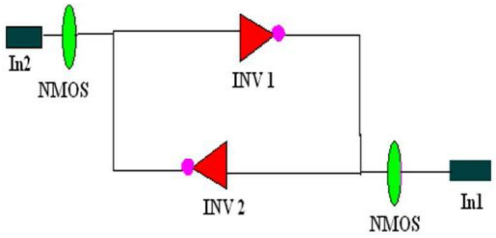

Fig1. *Cross-coupled inverters SRAM memory cell [3]*

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Non-volatile SRAM -Non-volatile SRAMshave standard SRAM functionality, but they save the data when the power supply is lost, ensuring preservation of critical information. Are used in a wide range of situations—networking, aerospace, and medical, among many others [4] -where the preservation of data is critical and where batteries are impractical.By transistor type-Bipolar junction transistor (used in TTL and ECL) – very fast but consumes a lot of power. MOSFET (used in CMOS) –low power and very common today. By function-Asynchronous – independent of clock frequency; data in and data out are controlled by address transition. Synchronous – all timings are initiated by the clock edge(s). Address, data in and other control signals are associated with the clock signals. By flip-flop type-Binary SRAM, Ternary SRAM.

CONVENTIONAL 6T CMOS SRAM

The conventional 6T SRAM cell is shown in Fig 1. The cell consists of 4 NMOS and 2 PMOS transistors. Structure can be visualized as two cross-coupled inverters with two NMOS transistors as word select. The write and read operations are:

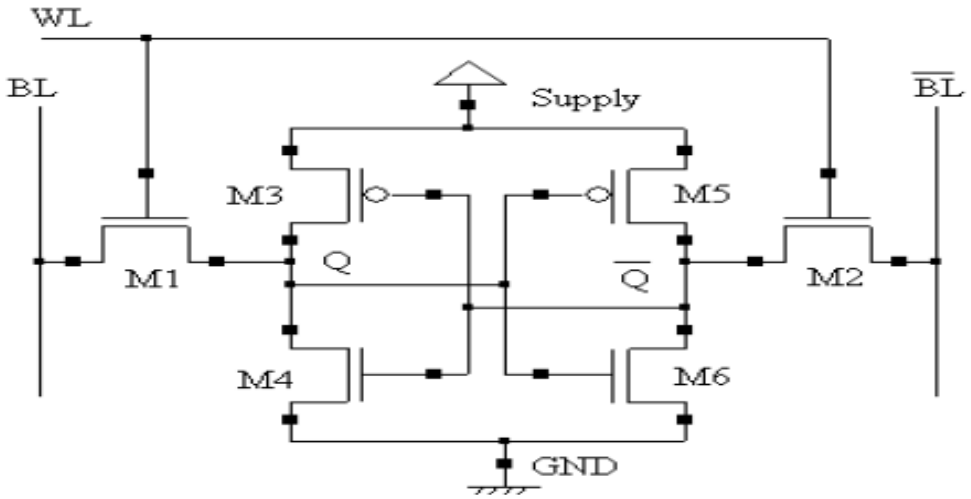

Fig2. *Conventional 6T SRAM Cell [5]*

Write Operation

In write operation two signals 'bI' and 'bIb' are generated from the input data such that 'bl' = data and 'bIb' = compliment of data. Then word line ('wI') is asserted which turns ON the access transistors m5 and m6 and the data will be written in the cell [7].

Read Operation

For read operation both bit lines ('bI' and 'bIb') are charged to a pre-charge voltage Vpre after that 'wI' is asserted, since the cell is already either in state '0' or in '1', then according to the state one line discharges to Gnd and a voltage difference is establishes between 'bI' and 'bIb' lines. Sense amplifier will sense this difference and stored bit will be available at the output of sense amplifier. From the working of 6T SRAM cell explained above, it is observed that power dissipation in SRAM can be divided into two parts. The first one is dynamic power, due to reading and writing of data, switching activity of transistors and charging and discharging of bit and bit-bar lines [6]. Second is when the cells are in steady state, because of leakage current of the MOS transistors.

LOW POWER SRAM CELL

Figure shows the write mode of low power SRAM cell. Word line is used for enabling the access transistors M1 and M2 for write operation. BL and $\overline{BL}$ lines are used to store the data and its compliment. For write operation one BL is High and the other bit line on low condition. In low power SRAM cell we introduced one Control signal transistor for controlling these transistors. But due to one more transistors area for low power SRAM cell is increased in comparison to Conventional approach. This control transistor uses control select signals which can be properly control the short circuit power dissipation. During write operation this transistor which has control signal works as in on condition. During read operation it will remain in off condition. When this transistor is in off condition will break the path which is in between V_{dd} and Ground.

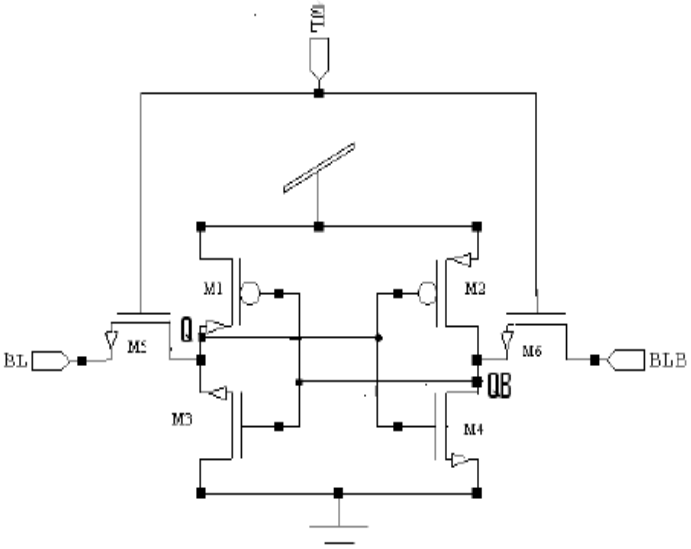

Fig3. *Low power 6-T SRAM cell*

SIMULATED SCHEMATICS USING TANNER TOOL

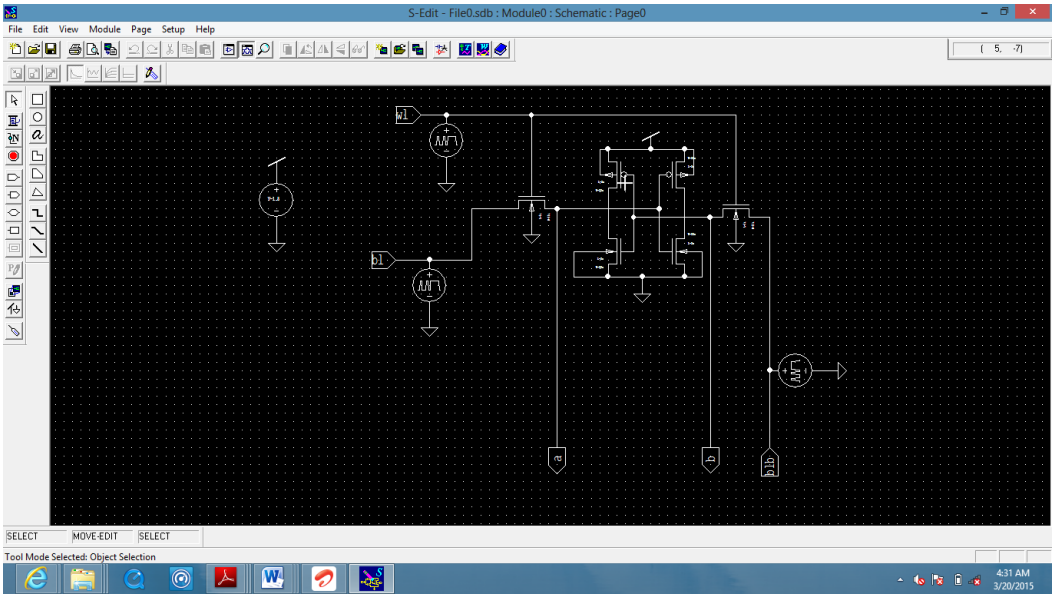

Fig4. *Schematic of 6T SRAM Cell*

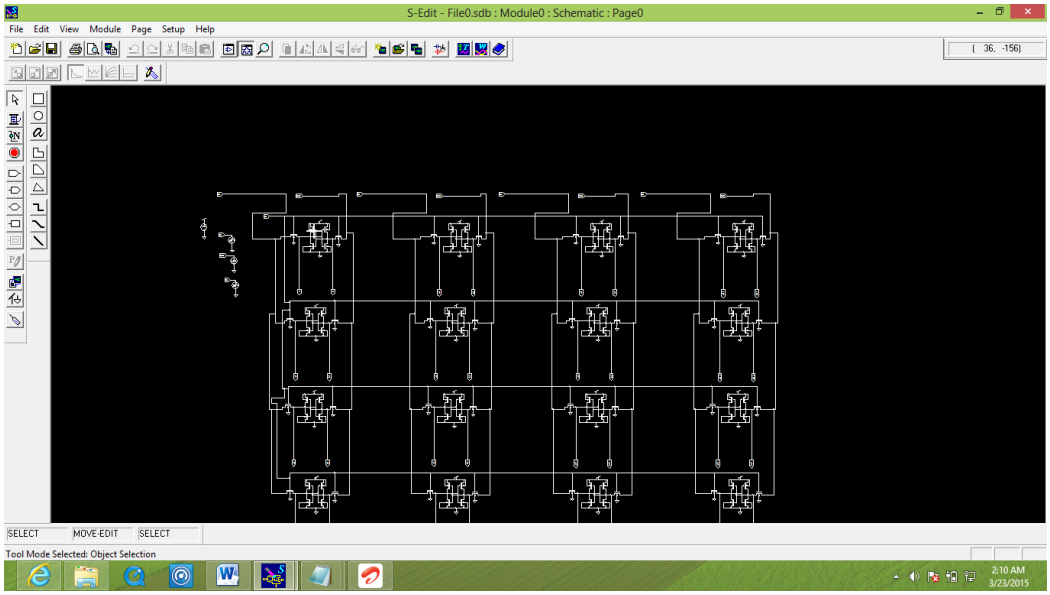

Fig5. *Schematic of16-bit memory SRAM Cell (i.e. 4 rows and 4 columns)*

SIMULATED WAVEFORMS RESULTS

The work has been developed usingTanner Tool version 7. And the waveform shows the Read/Write Waveforms of SRAM Cell at different technologies. Here, v(wl) v(blb) v(bl) are the inputs and v(a) v(b) are the outputs.

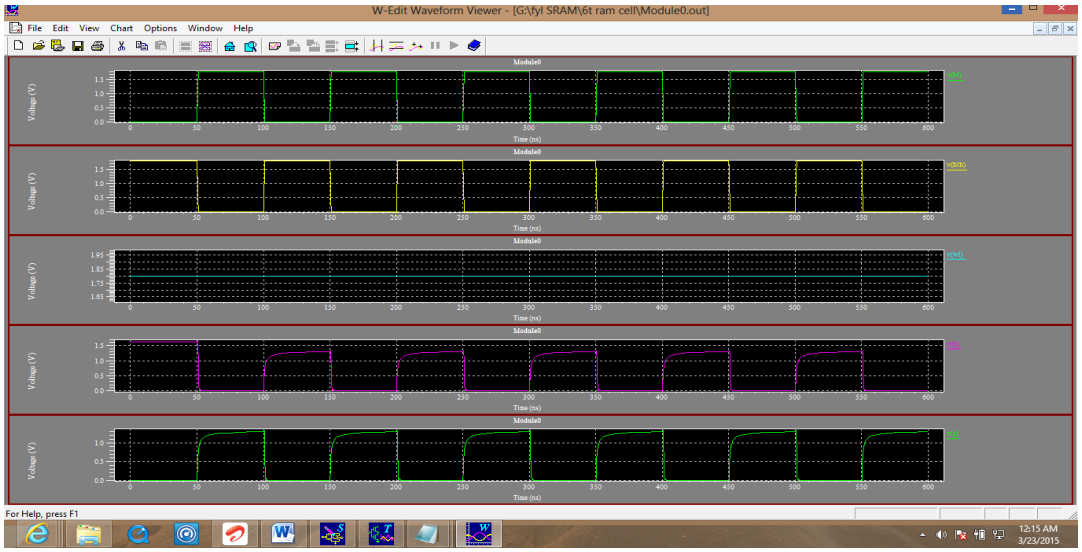

Fig6. *Read/Write Waveforms of 6T SRAM Cell at 90nm*

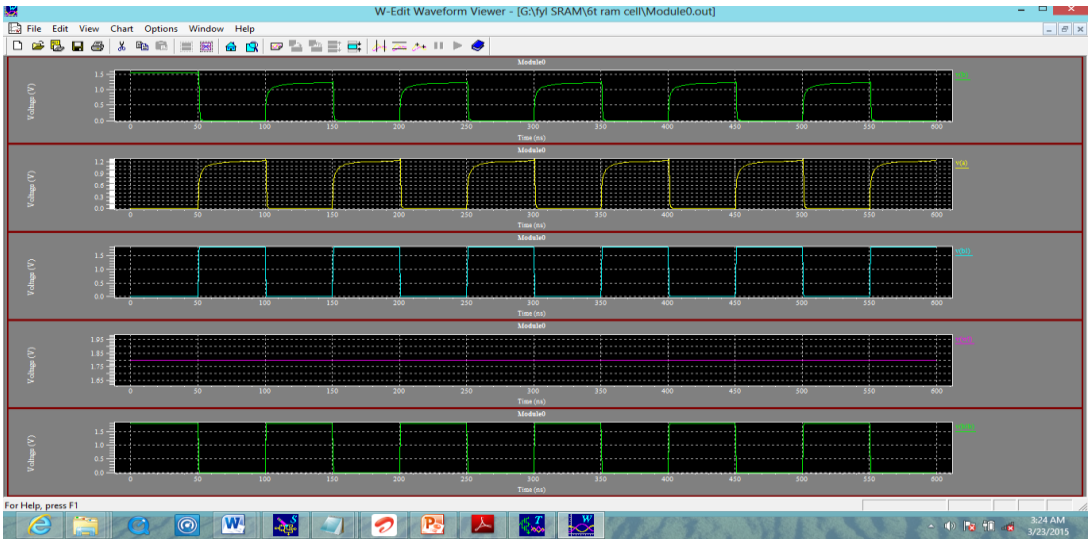

Fig7. *Read/Write Waveforms of 6T SRAM Cell at 90nm*

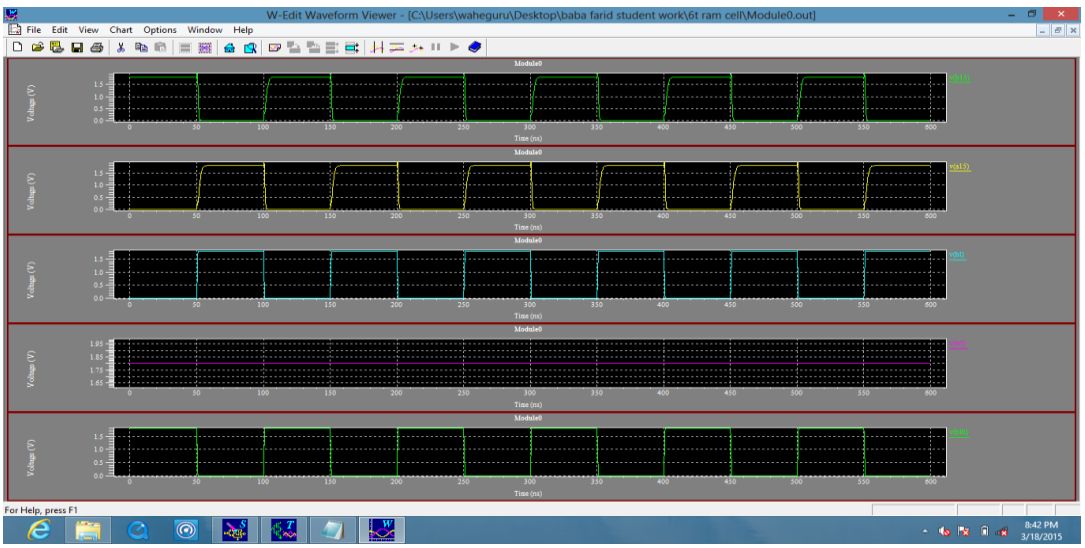

Fig8. *Read/Write Waveforms of 16-bit SRAM Cell at 90nm*

Fig9. *Read/Write Waveforms of 16-bit SRAM Cell at 180nm*

RESULTS AND COMPARATIVE ANALYSIS

All memory cells are simulated using T-SPICE 7.1v. In this section, comparison based results are presented in following tables. These results have been obtained from simulation of 6T memory cell in asymmetric configuration at the different technologies. And simulation of 16-bit SRAM memory cell in asymmetric configuration at the different technologies.

Table1. *Simulation results of 6T SRAM Cell for area, power and delay.*

Design style	No. of transistors	Technology file (µm)	Avg. power consumptions (watts)	Prop. Delay at a15 (sec)	Prop. Delay at b15 (sec)
SRAM	6	0.90	$2.94x10^{-5}$	$5.008x10^{-7}$	$5.007x10^{-7}$
SRAM	6	0.18	$4.11x10^{-5}$	$5.008x10^{-7}$	$5.51x10^{-7}$

Table2. *Simulation results of 16-bit SRAM Cell for area, power and delay.*

Design style	No. of transistors	Technology file (µm)	Avg. power Consumptions (watts)	Prop. delay at a15 (sec)	Prop. delay at b15 (sec)
SRAM	96	0.90	$6.14x10^{-4}$	$9.15x10^{-10}$	$9.15x10^{-10}$
SRAM	96	0.18	$7.59x10^{-4}$	$1.07\ x10^{-10}$	$1.07\ x10^{-10}$

CONCLUSION

Most of the developed low-power SRAM techniques are used to reduce only read power. Since, in the SRAM cell, the write power is generally larger than read power. We have proposed an SRAM cell to reduce the power in write operation by introducing two tail Transistors in the Pull-down path for reducing leakages.

In this paper the proposed cells utilize single bit line (BL) for write operation resulting in reduction of dynamic power. The 16-bit SRAM cell power dissipation on different technologies is compare with 6T SRAM cell. The comparisons of simulated results for all cases are shown in table-1 and 2.

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