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VLSI Modelling of High Speed Area Efficient Encoding Technique in Dedicated Short Range Communication Application Systems

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ABSTRACT

The dedicated short-range communication (DSRC) is an emerging technique to push the intelligent transportation system into our daily life. The DSRC standards generally adopt FM0 and Manchester codes to reach dc-balance, enhancing the signal reliability. Nevertheless, the coding-diversity between the FM0 and Manchester codes seriously limits the potential to design a fully reused VLSI architecture for both. In this paper, the similarity-oriented logic simplification (SOLS) technique is proposed to overcome this limitation. The SOLS technique improves the hardware utilization rate from 57.14% to 100% for both FM0 and Manchester encodings. The performance of this paper is evaluated on the post layout simulation in Taiwan Semiconductor Manufacturing Company (TSMC) 0.18-μm 1P6M CMOS technology. The maximum operation frequency is 2 GHz and 900 MHz for Manchester and FM0 encodings, respectively. The power consumption is 1.58 mW at 2 GHz for Manchester encoding and 1.14 mW at 900 MHz for FM0 encoding. The core circuit area is 65.98 × 30.43 μm2. The encoding capability of this paper can fully support the DSRC standards of America, Europe, and Japan. This paper not only develops a fully reused VLSI architecture, but also exhibits an efficient performance compared with the existing works.

Keywords: Dedicated short-range communication (DSRC), FM0, Manchester, VLSI.

INTRODUCTION

Dedicated Short Range Communication (DSRC) is a protocol used for communication for a short range of distance, say a few hundred meters through a dedicated channel. It is used to introduce intelligent transport system into our day to day life. The DSRC communication aids in both vehicle to vehicle communication as well as vehicle to roadside communication. The vehicle to vehicle communication mainly deals with the collision alarms, hard break warnings etc. At the same time the vehicle to infrastructure communication includes the Electronic Toll Collection (ETC), highway-rail intersection warning, in vehicle signing etc. However the primary motivation of the DSRC communication channel is collision detection and vehicular safety. In addition to it, it also aids in smooth traffic control. The DSRC equipment mainly consists of three modules namely; base band processors, RF front end and the microprocessors. The microprocessors are responsible for scheduling the tasks of base band processing and RF front end and intercept the instructions. The RF front end takes care of the transmission and reception of data. Finally main function of the base band processing includes modulation, error correction, clock synchronization, and encoding. For the purpose of encoding data, normally an FM0 or Manchester encoding are used so as to reduce the chances of occurrence of noise in the channel when it is left idle. When a system that can be reused between both the FM0 and the Manchester encoding is implemented, the hardware utilization rate is reduced thereby reducing the efficiency. This in turn affects the performance of the system. Hence a new method of designing a reusable VLSI architecture is proposed. This novel method of designing called the Similarity Oriented Logic Simplification (SOLS) improves the hardware utilization rate of the reusable architecture thereby improving the performance and area footage.

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RELATED TECHNOLOGIES

DSRC Protocol

Dedicated short range communication (DSRC) is a fast, short to mid range, wireless technology. It enables one way or two way communication between vehicles or between vehicles and roadside. It is to used make streets safer, travel easier and minimizes the impact vehicles have on the environment. It provides vehicles and infrastructure the ability to communicate with each other at a rate of 10 times per second. [1] In DSRC communication, the most important concern is collision detection. Each DSRC equipped vehicle broadcasts its basic information including speed, trajectory, location etc to a short range of distance, say a few hundred meters. All other DSRC equipped vehicles in the vicinity receives this message. Later on this message is decoded by the receiver vehicles and a caution or warning may be issued to the driver. This can be issued audibly, visually or haptically [3]. The DSRC communication is based on direct communication between vehicles and hence does not need networking. Therefore it is also referred to as single hop. This type of communication can also be referred to as uncoordinated broadcast messaging. Each DSRC equipped vehicles can extend this network to its neighbors and hence this network can grow unbounded. In case of safety, privacy is also an important concern. Therefore all safety communications are carried out in the control channel only. The safety communication involves two types of messages:

- Routine safety messages: These are status messages including change of speed, location, etc that are regularly sent by the vehicle.
- Event safety messages: These are messages that signify an event like a hard brake.

METHODOLOGY

FM0 Encoding

FM0 encoding is also a type of Non-Return to Zero code. It is also used to represent the binary signals in a digital system. In FM0 encoding, even though the data stream does not encounter transition, the encoded signal experiences a transition for every clock cycle. The FM0 encoding can be specified by using the three basic rules[1]. They are as follows:

1. There should be transition for every logic zero input within a clock cycle.
2. There should be no transition for logic one input.
3. There should be a transition after every clock cycle irrespective of the input data.

These rules can be better be explained by using the diagram (Fig 2).

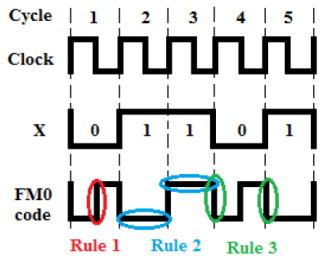

Figure2. *FM0 encoding*

FM0 encoding can be realized by using two flip-flops and also multiplexers. The FM0 encoding can be implemented by using the block diagram as shown below in fig 3. In the following block diagram, A(t) and B(t) signifies the two states.

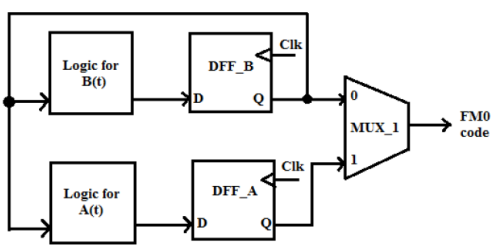

Figure3. *FM0 encoder*

Manchester Encoding

One of the most common data coding methods used today is Manchester encoding. Manchester coding gives a way of adding the data rate clock to the message to be used at the receiving end. To represent the binary values 1 and 0 in digital system, the Manchester codes are used. Manchester code represents binary values by a transition rather than a level. Manchester coding states that there will always be a transition of the message signal at the mid-point of the data bit frame. What occurs at the bit edges depends on the state of the previous bit frame and does not always produce atransition. A logical 1 is defined as a mid-point transition from low to high and a 0 is a mid-point transition from high to low.[1] An example of a Manchester encoding is shown below in Fig 4.

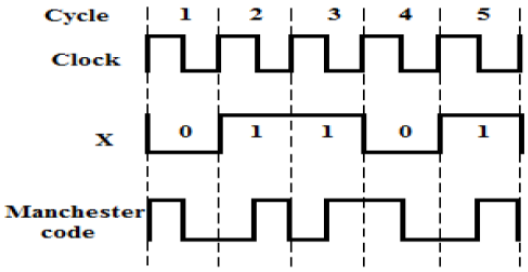

Figure4. *Manchester Encoding*

The Manchester encoding can be implemented using an XOR gate where the clock signal and the data signal are XORed together to obtain the encoded data as shown in the diagram below (Fig 5.)

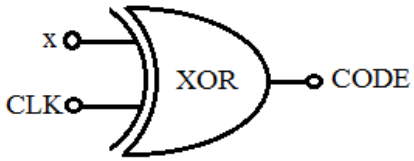

Figure5. *Manchester encoder*

SOLS Technique

Normally DSRC encoders make use of both the FM0 and the Manchester encoding. Hence both the encoders can be combined together to form a reusable encoder. Such a reusable encoder can be illustrated as shown in the figure 6.

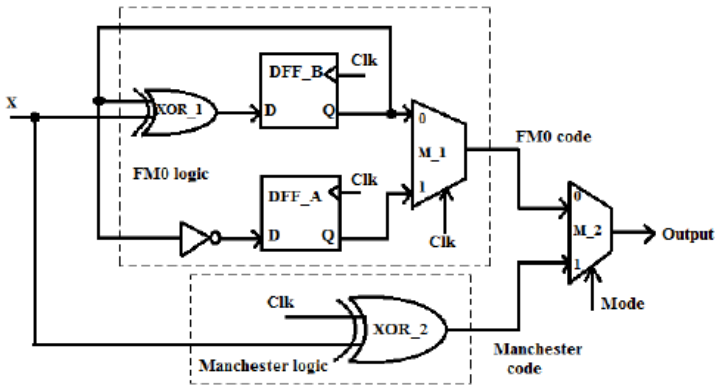

Figure6. *Reusable encoder*

This block diagram can be further simplified using the SOLS technique. The SOLS encoder consists of mainly two methods, area compact retiming and the balance logic simplification.

SIMULATION RESULTS

The SOLS written in verilog compiled and simulation using Xilinx ise. The circuit simulated and synthesized. The simulated result for SOLS

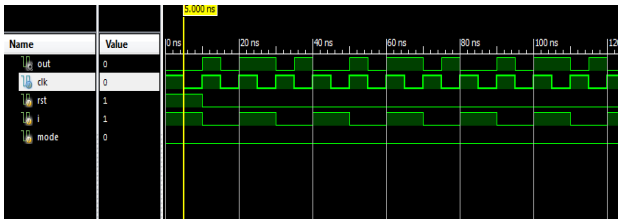

Fig7. *Simulation Result of FMO*

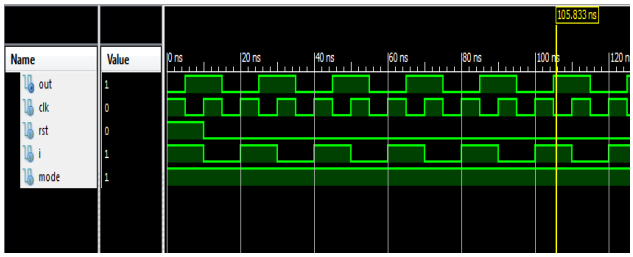

Fig7. *Simulation Result of* **:** *Manchester Encoding*

CONCLUSION

The coding-diversity between FM0 and Manchester encodings causes the limitation on hardware utilization of VLSI architecture design. A limitation analysis on hardware utilization of FM0 and Manchester encodings is discussed in detail. In this paper, the fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings is proposed. The SOLS technique eliminates the limitation on hardware utilization by two core techniques: area compact retiming and balance logic-operation sharing. The area-compact retiming relocates the hardware resource to reduce 22 transistors. The balance logic-operation sharing efficiently combines FM0 and Manchester encodings with the identical logic components. This paper is realized in TSMC 0.18-μm 1P6MCMOS technology with an outstanding device efficiency. The maximum operation frequency is 2 GHz and 900 MHz for Manchester and FM0 encodings, respectively. The power consumption is 1.58 mW at 2 GHz for Manchester encoding and 1.14 mW at 900 MHz for FM0 encoding. The core circuit area is 65.98 × 30.43 μm2. The encoding capability of this paper can fully support the DSRC standards of America, Europe, and Japan. This paper not only develops a fully reused VLSI architecture, but also exhibits a competitive performance compared with the existing works.

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