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Design of Low Power 8-Bit Shift Register using PFF

Anuja Kakde

M.Tech (VLSI), Sri Devi Women's Engineering College

Dr.BL.Malleshwari, M.S.,Ph.d

Principal, Sri Devi Women's Engineering College

ABSTRACT

In this brief, Design of low-power 8-bit shift register is done by using flip-flop (FF) design featuring an explicit type pulse-triggered structure based on a signal feed-through scheme is presented. The proposed design successfully solves the long discharging path problem in conventional explicit type pulse-triggered FF (P-FF) designs and achieves better speed and power performance. Using 8-bits of PFF 8-Bit shift register is designed. Based on post-layout simulation results using TSMC CMOS 90-nm technology, the proposed design outperforms the conventional P-FF design data-close-to-output (ep-DCO) by 8.2% in data-to-Q delay. In the mean time, the performance edges on power and power delay product metrics are 22.7% and 29.7%, respectively.

The objective of the project is to design 8-bit shift register using pulse triggered flip flop with signal feed through scheme which consumes less power and delay will be reduced.

In this project different implicit and explicit type flip flops are simulated in Hspice using 180nm technology whereas proposed design circuit is simulated in Hspice using 90nm technology.

Keywords: Flip-flop (FF), low power, pulse-triggered, signal feed through scheme,TSPC

INTRODUCTION

P-FFs, in terms of pulse generation, can be classified as an implicit or an explicit type. In an implicit type P-FF, the pulse generator is part of the latch design and no explicit pulse signals are generated. In an explicit type P-FF, the pulse generator and the latch are separate. Without generating pulse signals explicitly, implicit type P-FFs are in general more power-economical. However, they suffer from a longer discharging path, which leads to inferior timing characteristics.

Pulse-triggered FF(P-FF), because of its single-latch structure, is more popular than the conventional transmission gate (TG) and master–slave based FFs in high-speed applications. Besides the speed advantage, its circuit simplicity lowers the power consumption of the clock tree system. A P-FF consists of a pulse generator for strobe signals and a latch for data storage. If the triggering pulses are sufficiently narrow, the latch acts like an edge-triggered FF. Since only one latch, as opposed to two in the conventional master–slave configuration, is needed, a P-FF is simpler in circuit complexity. Hence the design of shift registers using P-FF will be power economical.

PROBLEM STATEMENT

In recent years many researchers worked on various designs of flip flops. The conventional master slave flip flop has more transistor count in its design and sensitive to clock jitter and also has large clock to output delay. Hence these designs are not power economical. To overcome these problems researches has worked on new design technique which is known as pulse triggered flip flops.

Objective of Project

- **Design of low power shift registers**

The low power shift registers serial-in serial-out, parallel-in serial-out, parallel-in parallel-out can be designed by using the proposed low power P-FF and its performance is compared with all implicit and explicit shift registers.

Software Required: Hspui A – 2008.03

PROPOSED 8-BIT SHIFT REGISTER

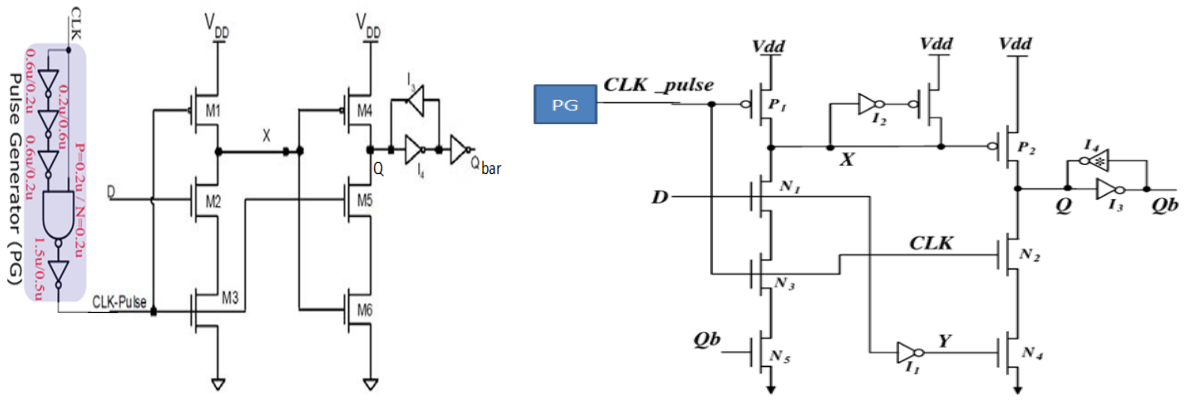
Conventional Explicit Type P-FF Designs

PF-FFs, in terms of pulse generation, can be classified as an implicit or an explicit type. In an implicit type P-FF, the pulse generator is part of the latch design and no explicit pulse signals are generated. In an explicit type P-FF, the pulse generator and the latch are separate [7]. Without generating pulse signals explicitly, implicit type P-FFs are in general more power-economical. However, they suffer from a longer discharging path, which leads to inferior timing characteristics. Explicit pulse generation, on the contrary, incurs more power consumption but the logic separation from the latch design gives the FF design a unique speed advantage. Its power consumption and the circuit complexity can be effectively reduced if one pulse generator is shares a group of FFs (e.g., an n-bit register). In this brief, we will thus focus on the explicit type P-FF designs only.

To provide a comparison, some existing P-FF designs are reviewed first. Fig. 1(a) shows a classic explicit P-FF design, named data-close- to-output (ep-DCO) [7]. It contains a NAND-logic-based pulse generator and a semidynamic true-single-phase-clock (TSPC) structured latch design. In this P-FF design, inverters I3 and I4 are used to latch data, and inverters I1 and I2 are used to hold the internal node X . The pulse width is determined by the delay of three inverters. This design suffers from a serious drawback, i.e., the internal node X is discharged on every rising edge of the clock in spite of the presence of a static input "1." This gives rise to large switching power dissipation. To overcome this problem, many remedial measures such as conditional capture, conditional precharge, conditional discharge, and conditional pulse enhancement scheme have been proposed [14]–[18]. Fig. 1(b) shows a conditional discharged (CD) technique [16]. An extra nMOS transistor MN3 controlled by the output signal Q_fdbk is employed so that no discharge occurs if the input data remains "1."

In addition, the keeper logic for the internal node X is simplified and consists of an inverter plus a pull-up pMOS transistor only.

Fig.1(c) shows a similar P-FF design (SCDFF) using a static conditional discharge technique [17]. It differs from the CDFF design in using a static latch structure. Node X is thus exempted from periodical precharges. It exhibits a longer data-to-Q (D-to-Q) delay than the CDFF design. Both designs face a worst case delay caused by a discharging path consisting of three stacked transistors, i.e., MN1–MN3. To overcome this delay for better speed performance, a powerful pull-down circuitry is needed, which causes extra layout area and power consumption. The modified hybrid latch flip-flop (MHLFF) [19] shown in Fig. 1(d) also uses a static latch. The keeper logic at node X is removed. A weak pull-up transistor MP1 controlled by the output signal Q maintains the level of node X when Q equals 0. Despite its circuit simplicity, the MHLFF design encounters two drawbacks. First, since node X is not predischarged, a prolonged 0 to 1 delay is expected. The delay deteriorates further, because a level-degraded clock pulse (deviated by one VT) is applied to the discharging transistor MN3. Second, node X becomes floating in certain cases and its value may drift causing extra dc power.



(a) (b)

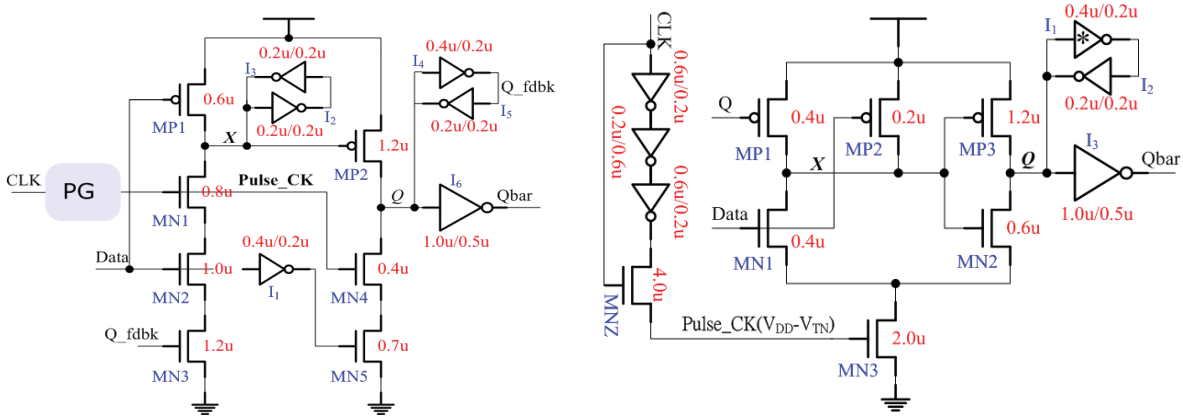


Fig1. *Conventional P-FF designs (a) ep-DCO (b) CDFF (c) Static-CDFF (d) MHLFF*

P-FF Design

Recalling the four circuits reviewed in Section II-A, they all encounter the same worst case timing occurring at 0 to 1 data transitions. Referring to Fig. 2(a), the PFF adopts a signal feed-through technique to improve this delay. Similar to the SCDFF design, the PFF also employs a static latch structure and a conditional discharge scheme to avoid superfluous switching at an internal node. However, there are three major differences that lead to a unique TSPC latch structure and make the proposed design distinct from the previous one. First, a weak pull-up pMOS transistor MP1 with gate connected to the ground is used in the first stage of the TSPC latch. This gives rise to a pseudo-nMOS logic style design, and the charge keeper circuit for the internal node X can be saved. In addition to the circuit simplicity, this approach also reduces the load capacitance of node X [20], [21]. Second, a pass transistor MNx controlled by the pulse clock is included so that input data can drive node Q of the latch directly (the signal feed-through scheme). Along with the pull-up transistor MP2 at the second stage inverter of the TSPC latch, this extra passage facilitates auxiliary signal driving from the input source to node Q. The node level can thus be quickly pulled up to shorten the data transition delay. Third, the pull-down network of the second stage inverter is completely removed. Instead, the newly employed pass transistor MNx provides a discharging path. The role played by MNx is thus twofold, i.e., providing extra driving to node Q during 0 to 1 data transitions, and discharging node Q during "1" to "0" data transitions. Compared with the latch structure used in SCDFF design, the circuit savings of the PFF include a charge keeper (two inverters), a pull-down network (two nMOS transistors), and a control inverter. The only extra component introduced is an nMOS pass transistor to support signal feed through. This scheme actually improves the "0" to "1" delay and thus reduces the disparity between the rise time and the fall time delays. In comparison with other P-FF designs such as ep-DCO, CDFF, and SCDFF, the PFF shows the most balanced delay behaviors.

When a clock pulse arrives, if no data transition occurs, i.e., the input data and node Q are at the same level, on current passes through the pass transistor MNx, which keeps the input stage of the FF from any driving effort. At the same time, the input data and the output feedback Q_fdbk assume complementary signal levels and the pull-down path of node X is off. Therefore, no signal switching occurs in any internal nodes. On the other hand, if a "0" to "1" data transition occurs, node X is discharged to turn on transistor MP2, which then pulls node Q high. However, with the signal feed-through scheme, a boost can be obtained from the input source via the pass transistor MNx and the delay can be greatly shortened. Although this seems to burden the input source with direct charging/discharging responsibility, which is a common pitfall of all pass transistor logic, the scenario is different in this case because MNx conducts only for a very short period.When a "1" to "0" data transition occurs, transistor MNx is likewise turned on by the clock pulse and node Q is discharged by the input stage through this route. Unlike the case of "0" to "1" data transition, the input source bears the sole discharging responsibility. Since MNx is turned on for only a short time slot, the loading effect to the input source is not significant. In particular, this discharging does not correspond to the critical path delay and calls for no transistor size tweaking to enhance the speed. In addition, since a keeper logic is placed at node Q, the discharging duty of the input source is lifted once the state of the keeper logic is inverted..

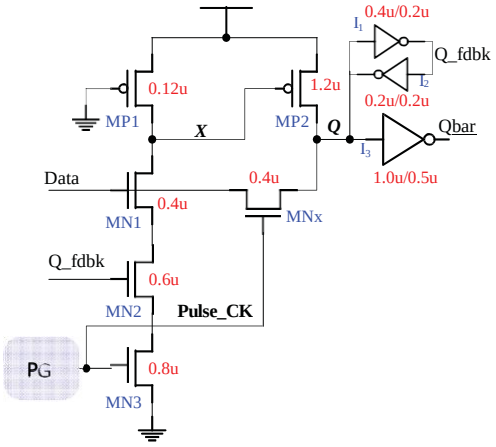


Fig2. *Schematic of the P-FF design*

Proposed Architecture (SHIFT REGISTER USING PFF)

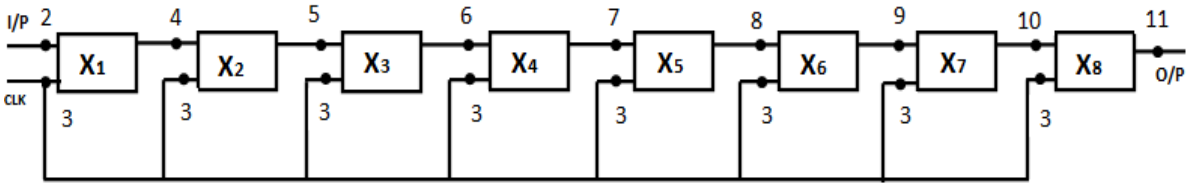


Fig3. *Block diagram of proposed shift register*

X = PFF(PULSE TRIGGERED FLIP-FLOP).

CLK = CLOCK.

Using PFF in fig.2 proposed 8-Bit shift register is designed. The inputs and outputs are as shown in block diagram in fig.3

RESULTS

Simulation Result

The performance of the P-FF design is evaluated against existing designs through post-layout simulations. The compared designs include four explicit type P-FF designs shown in Fig.1, an implicit type P-FF design named SDFF(statc CDFF), EP-DCO (data close to output flip flop), CDFF (conditional discharge flip flop), MHLFF (modified hybrid latch flip flop). A conventional CMOS NAND-logic-based pulse generator design with a three-stage inverter chain [as show in Fig. 1(a)] is used for all P-FF designs except the MHLFF design, which employs its own pulse generation circuitry as specified in Fig.1(d).

The target technology is the TSMC 90-nm CMOS process. Since pulse width design is crucial to the correctness of data capture as well as the power consumption [10]–[13], the transistors of the pulse generator logic are sized for a design spec of 120 ps in pulse width in the TT case. The sizing also ensures that the pulse generators can function properly in all process corners. With regard to the latch structures, each P-FF design is individually optimized subject to the product of power and D-to-Q delay. To mimic the signal rise and fall time delays, input signals are generated through buffers. Since the PFF requires direct output driving from the input source, for fair comparisons the power consumption of the data input buffer (an inverter) is included. The output of the FF is loaded with a 20ff capacitor. An extra loading capacitance of 3ff is also placed at the output of the clock buffer. The delay and power comparison are shown in table. After all these comparison it is concluded that power and delay used in PFF is less compared to other conventional flip flops. Hence PFF is cascade to design low power 8-bit shift register.

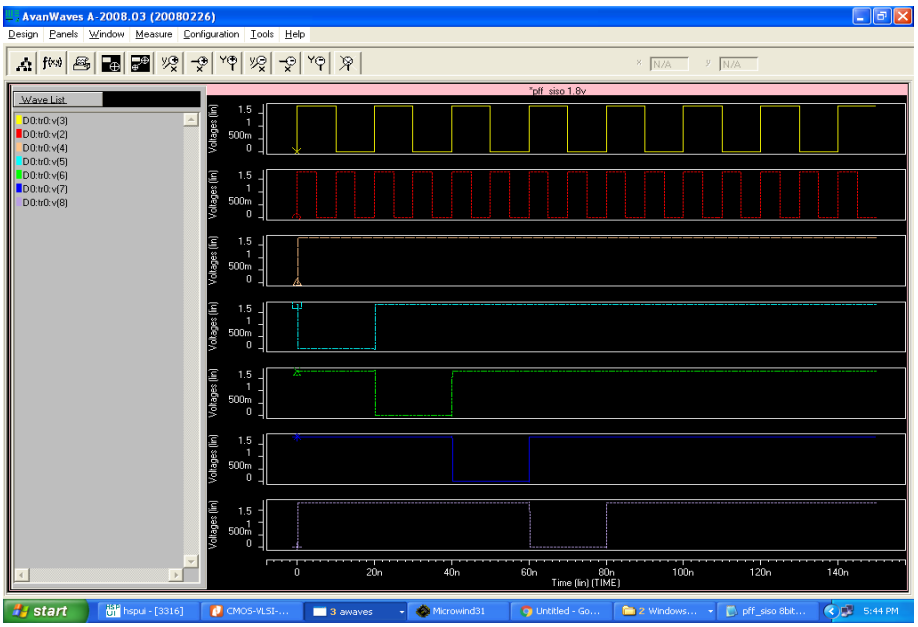


Fig. *Simulation result of Proposed shift register using pulse triggered flipflop*.

Comparison Table

Table. *Power & Delay comparison table for conventional flip flops with PFF*

Flip-Flop design	Power $(\mu watts)$	Delay
Ep-Dco	28.4	11.45p
CDFF	31.8	315.74p
Static-CDFF	28.6	179.16p
MHLFF	11.2	191.78p
P-FF	10.9	2.52p
Shift register using P-FF	180	139.6p

APPLICATIONS

- Shift registers can also function as delay circuits.
- One of the most common uses of a shift register is to convert between serial and parallel interfaces
- SIPO registers are commonly attached to the output of microprocessors when more General Purpose Input/Output pins are required than are available
- Shift registers are often used for the purpose of saving pins on a microcontroller

ADVANTAGES

- Power consumption is reduced.
- Area is optimized compared to other designs.
- Circuit complexity is reduced.

CONCLUSION

A new pulse triggered FF with an explicit pulse generator is used with modified TSPC latch structure incorporating a mixed design style consisting of a pass transistor and a pseudo-nMOS logic to design low power proposed shift register. The key idea was to provide a signal feed through from input source to the internal node of the latch, which would facilitate extra driving to shorten the transition time and enhance both power and speed performance.

The simulation results obtained prove that PFF design is far better than the other conventional flip flops shown in this paper.

The power is reduced since the pulse generator is shared with flip flops. Hence the shift registers designed with all flip-flop designs also prove that shift registers built with pulse triggered flip flop is a better low power design.

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