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Voltage Sag Compensation Method for Z Source Impedance Based Interline Dynamic Voltage Restorer

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ABSTRACT

The Interline DVR (IDVR) proposed in this paper provides a way to compensate the voltage deviation caused in a feeder. The IDVR consists of several DVRs connected to different distribution feeders in the power system sharing common energy storage. A new topology based on Z-source inverter is presented in order to enhance the voltage restoration property of dynamic voltage restorer. The modeling of Z-source based IDVR is carried out component wise and their performances are analyzed using MATLAB software. The simulation results shows that the control technique is very effective and yields excellent compensation for voltage sag/swell mitigation.

Keywords: *Interline Dynamic Voltage Restorer (IDVR), Dynamic Voltage Restorer (DVR), Pulse Width Modulation (PWM), Total Harmonic Distortion (THD),* (IDVR), Z source Inverter (ZSI), Pulse Width Modulation(PWM), Total Harmonic Distortion (THD)

INTRODUCTION

The need of the electrical power is increasing and simultaneously the problems while transmitting the power through the distribution system are also increasing. Voltage fluctuations are considered as one of the most severe power quality disturbances to be dealt with. Even a short-duration voltage fluctuation could cause a malfunction or a failure of a continuous process. There are several types of voltage fluctuations that can cause the systems to malfunction, including surges and spikes, sag, swell, harmonic distortions, and momentary disruptions. Among them, voltage sag and swell are the major power-quality problems.

The concept of Interline Dynamic Voltage Restorer (IDVR) where two or more voltage restorers are connected such that they share a common DC-link is similar to the Interline Power Flow Controller (IPFC) concept. In this paper, a two-line IDVR system is explained which employs two DVRs connected to two different feeders originating from two grid substations, could be of the same or different voltage level. However the DC-link of these two DVRs could be connected to a common DC-link. This would cut down the cost as sharing a common DC-link reduces the DC-link storage capacity significantly compared to that of a system whose loads are protected by clusters of DVRs with separate energy storages. When one of the DVRs compensates for voltage sag or swell produced, the other DVR in IDVR system operates in power-flow control mode. This is to replenish DC-link energy storage, which is depleted due to the power taken by the DVR working in the voltage-sag/swell compensation mode. The DVR is operated in such a fashion that it does not supply or absorb any active power during the steady-state operation [1]. It is desirable to have a minimum VA rating of the DVR, for a given system without compromising compensation capability [2]. Control algorithm for dynamic voltage restorer (DVR) to improve voltage quality problems such as voltage sags/swells in distribution systems has been proposed [3].

The DVR consists of three inverters sharing the same DC link via a capacitor bank. Each inverter has an individual inner control loop for generating the gate signals for the switches [4]. The Pulse-width modulation of Z-source inverter has recently been proposed as an alternative power conversion concept as they have both voltage buck and boost capabilities [5].

The voltage-restoration process involves real-power injection into the distribution system, the capability of a particular DVR topology, especially for compensating long-duration voltage sags, depends on the energy storage capacity of the DVR [6]. The main factor which limits capabilities of a particular DVR in compensating long-duration voltage sags is the amount of stored energy within the restorer [7]. The modeling and simulation of DVR and IDVR is presented [8 -14]. The literature [1] to [14] does not deal with ZSI based IDVR system. An attempt is made in the present work to model IDVR system using the blocks of MATLAB simulink.

PRINCIPLES OF OPERATION OF IDVR

The IDVR system consists of several DVRs in different feeders, sharing a common DC-link. A two-line IDVR system shown in Figure 1 employs two DVRs are connected to two different feeders where one of the DVRs compensates for voltage sag or swell produced, the other DVR in IDVR system operates in power-flow control mode.

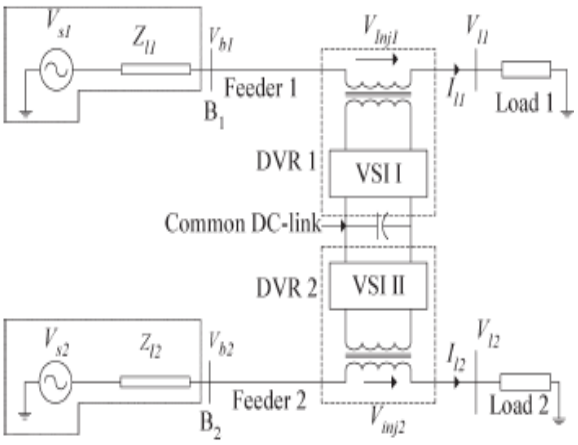

Figure1. *Schematic diagram of an IDVR*

Elements of an IDVR System

The upstream generation-transmission system is applied and the two feeders can be considered as two independent sources. These two voltage sources Vs1 and Vs2 are connected in series with the line impedances Zl1 and Zl2 which is in-turn connected to the buses B1 and B2 as in Figure 1. The DVR is connected in series with the feeder and the DVRs across different feeders are connected by a common DC-link. The common DC-link indicated between the two DVRs is a large capacitor that acts as a voltage storage device. A Z-Source Inverter (ZSI) is present which boosts the DC voltage. This DC voltage is inverted to AC voltage which is injected to the transformer. The load across each feeder is connected in series to the DVR, where Vl1 and Vl2 are the voltages across the load.

Energy Storage Requirement of an IDVR System

The injection of an appropriate voltage needs a certain amount of real and reactive power which must be supplied by the DVR. Supply of real power is met by means of an energy storage facility connected in the DC-link. Large capacitors are used as a source of energy storage in most of the DVRs. Generally, capacitors are used to generate reactive power in an AC power system. However, in a DC system, capacitors can be used to store energy. When the energy is drawn from the energy storage capacitors, the capacitor terminal voltage decreases. Hence, large capacitors in the DC-link energy storage are needed to effectively mitigate voltage sag/swell of large depths and long durations.

Z-Source Inverter

Z-source inverter has X-shaped impedance network on its DC side, which interfaces the source and inverter H-bridge. It facilitates both voltage-buck and boost capabilities. The impedance network composed of split inductors and two capacitors. The supply can be DC voltage source or DC current source or AC source. Z-source inverter can be of current source type or voltage source type. Figure 2 shows the general block diagram of Z-Source inverter.

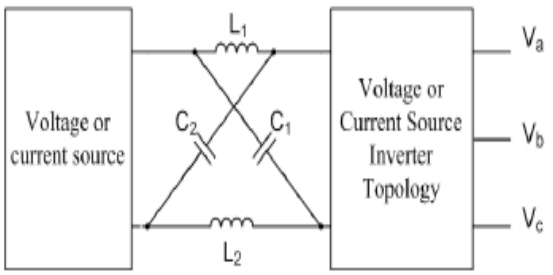

Figure2. *Block Diagram of Z-Source Inverter*

Modulation Technique for Pulse Generation

Z-Source inverter operation is controlled by multiple pulse width modulation. The output of the Z-Source inverter is controlled by using pulse width modulation, generated by comparing a triangular wave signal with an adjustable DC reference and hence the duty cycle of the switching pulse could be varied to synthesize the required conversion.

As shown in Table I, the single-phase Z-Source inverter has five switching modes. Two active modes in which the dc source, voltage is applied to load, two zero modes in which the inverter's output terminals are short circuited by S1 and S3 or S2 and S4 switches and a shoot-through mode which occurs as two switches on a single leg are turned on.

Table1. *Switching Modes*

S_4	S_3	S_2	S_1	Switching mode
1	0	0	1	Active mode
0	1	1	0	
0	1	0	1	Zero mode
1	0	1	0	

Applying a distinctive PWM method is necessary for ZSI considering the defined operational modes. The equivalent circuits of rectifier fed ZSI in shoot-through and active modes are presented in Figs. 3and 4 respectively. In a symmetric impedance network, the following equations are valid:

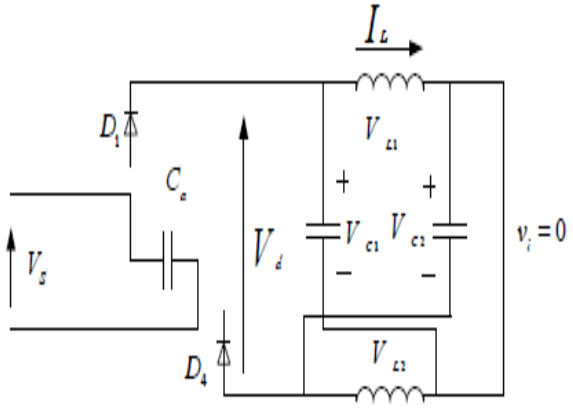

Figure3. *Shoot through mode*

$$C_1 = C_2 = C \quad (1)$$

$$L_1 = L_2 = L \quad (2)$$

$$I_{L1} = I_{L2} = I_L \quad (3)$$

$$V_{C1} = V_{C2} = V_C \quad (4)$$

The voltage of capacitors in a symmetric impedance network is as follows:

$$V_i = \beta V_{dc} \quad (5)$$

$$\beta = 1/[1 - 2(T_0/T) \quad (6)$$

Where, T0 and T show the shoot-through mode application period and switching period, respectively. Also, the following relation is valid in symmetric impedance networks:

$$V_i = 2V_C - V_{dc} \quad (7)$$

It should be noted that the relations mentioned above are extracted by averaging the ZSI operational modes. The shunt full bridge rectifier with the input capacitor Ca which feeds the impedance network is shown in Figure 4. During the commutation between diodes, it is possible to face with surge voltage due to line inductance and shoot-through mode operation. The input capacitor is used to suppress this surge voltage. Diodes D1 and D4 are turned on if the input voltage of rectifier is positive. Diodes D3 and D2 are turned on if the input voltage of rectifier is not positive.

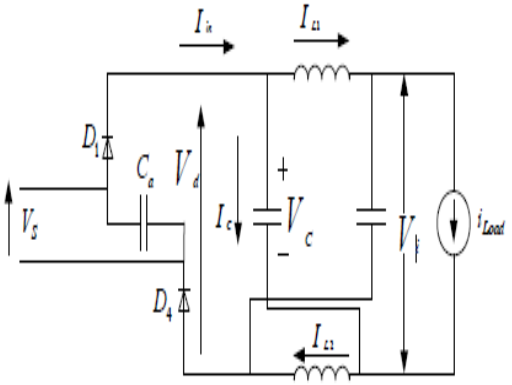

Figure4. *Active mode*

The following is obtained according to that equivalent circuit:

$$V_d = V_{L1} + V_{C2} \quad (8)$$

$$V_{L1} = V_{C1} \quad (9)$$

Where Vd is the impedance network input voltage. Considering (4), (8) and (9), the following relation is obtained:

$$V_d = 2V_C \quad (10)$$

In shoot-through mode operation, the rectifier is not able to inject current and energy to impedance network. Fig. 6 shows the equivalent circuit of ZSI in active mode. Considering Fig. 6, the following relation is obtained

$$V_d = V_s(t) - 2V_g \quad (11)$$

SIMULATION RESULTS OF AN IDVR

The simulink model of an IDVR for voltage sag compensation is shown in Figure 5. For a closed loop control, the output voltage from the load across the load is rectified to give a DC voltage. This DC voltage is controlled via PI controller.

The error is used and the driving pulse is generated. This pulse is fed to the rectifier which therefore yields in the injection of voltage. The injected voltage of the DVR depends on the accuracy and dynamic behavior of the pulse width-modulation.

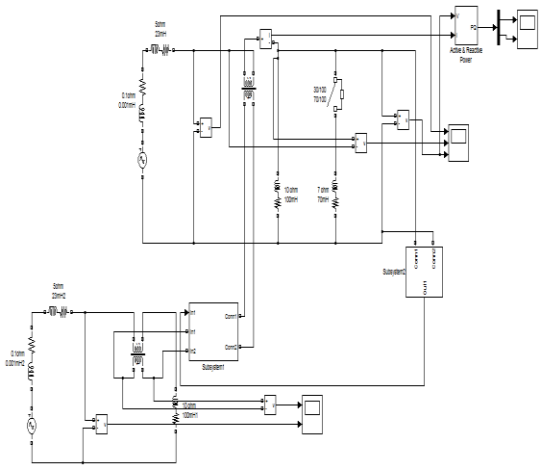

Figure5. *Simulation circuit of voltage sag / swell*

The Figure 6 shows the response of voltage sag compensation in a closed loop control of a two feeder IDVR system. Figure 7 shows the real and reactive power obtained across Feeder$_1$. Both the real and reactive power is increased when there is an increase in the load. The Figure 8 shows the Total Harmonic Distortion (THD) is 4.38% for a 20% of voltage sag

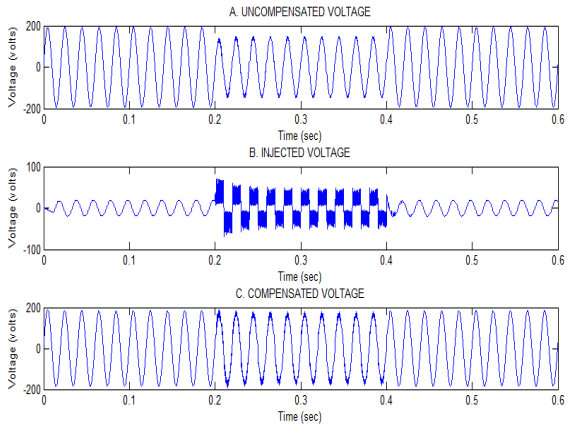

Figure6. *Response of IDVR at 20% voltage sag*

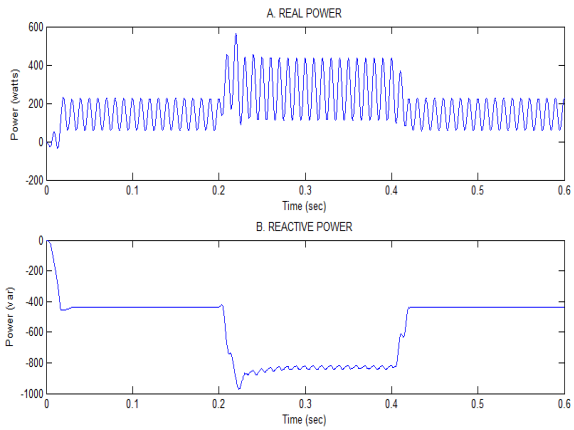

Figure7. *Real and reactive powers of feeder$_1$*

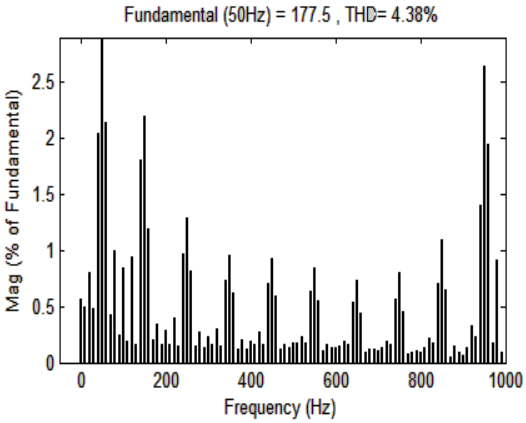

Figure8. *FFT analysis of output voltage*

The Figure 9 shows the response of voltage swell compensation in a closed loop control of two feeder IDVR system. Figure 10 shows the real and reactive power obtained across feeder1. The Figure 11 shows the Total Harmonic Distortion (THD) is 5.5% for a 20% of voltage swell.

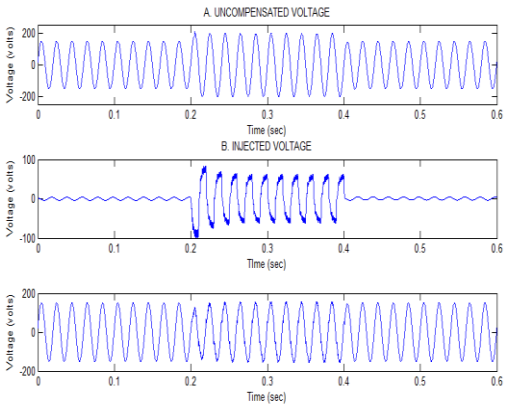

Figure9. *Response of IDVR at 20% voltage swell*

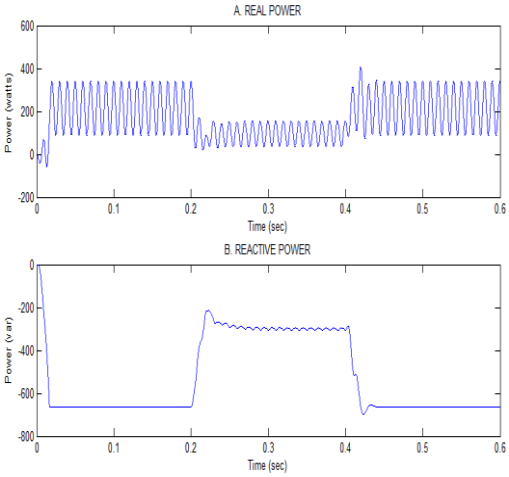

Figure10. *Real and reactive powers of feeder$_1$*

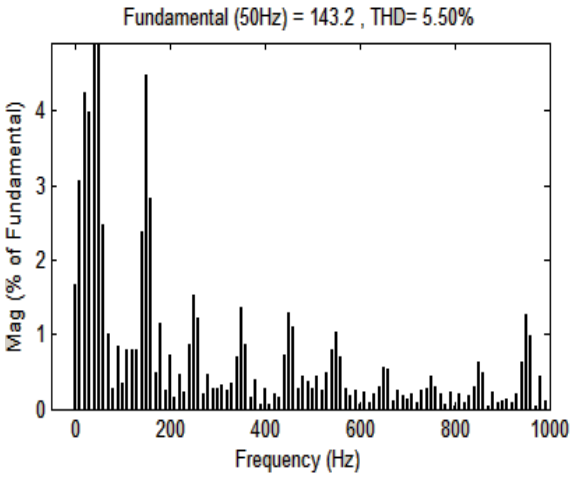

Figure11. *FFT analysis of output voltage*

CONCLUSION

In this paper voltage sag/swell compensation using Z-Source inverter based IDVR is considered. The modeling and simulation of closed loop control of voltage sag/swell mitigation were carried out using MATLAB software. The simulation results show that the developed control technique with proposed single phase IDVR is simple and efficient.

REFERENCES

[1] Anil Kumar. R, Siva Kumar. G, "Compensation of Voltage Sags and Harmonics with Phase-Jumps through DVR with minimum VA rating Using Particle Swarm Optimization", *Proceedings of World Congress on Nature and Biologically Inspired Computing*, 2009, pp. 1361-1366.

[2] Mahinda Vilathgamuwa.D, "A Novel Technique to Compensate Voltage Sags in Multiline Distribution System—The Interline Dynamic Voltage Restorer", *IEEE transactions on Industrial Electronics*, Vol. 53, No. 5, 2006, pp.1603-1611.

[3] Mahinda Vilathgamuwa. D, "Interline Dynamic Voltage Restorer: A Novel and Economical Approach for Multiline Power Quality Compensation", *IEEE transactions on Industry Applications*, Vol. 40, No. 6, 2004, pp.1678-1685.

[4] Usha Rani P, "Voltage swell compensation in an interline dynamic voltage restorer", *Joul of Sci & Indl Resh*, Vol.73, No.1, 2014, pp.29-32.

[5] Usha Rani P. and Rama Reddy S, "Modeling and Simulation of Interline Dynamic Voltage Restorer for Voltage Sag/Swell Compensation", *Journal of Electrical Engineering*,Vol.11, No.3, 2011, pp.166-172.

[6] Usha Rani P. and Rama Reddy S, "Digital Simulation of a Dynamic Voltage Restorer System", *Annals of Dunarea De Jos University of Galati, Electrotechnics, Electronics, Automatic Control, Informatics*, Vol. 32, No. 2, 2009, pp. 64-68.

[7] Usha Rani P. and Rama Reddy S, "Digital Simulation of an Interline Dynamic Voltage Restorer for Voltage Compensation", *International conference on Computer, Communication and Electrical Technology IEEE Xplore ICCCET*, 2011, pp. 133-139.

[8] Usha Rani P. and Rama Reddy S, "Modeling and Simulation ZSI based DVR for voltage compensation", *International conference on Computer, Communication and Electrical Technology IEEE Xplore ICCCET*, 2011, pp. 90-96.

[9] Usha Rani P. and Rama Reddy S, "Voltage sag / swell compensation in an interline dynamic voltage restorer", *International conference on Emerging Trends in Electrical and Computer Technology, IEEE Xplore ICETECT*, 2011, pp. 309-314.

[10] Usha Rani P. and Rama Reddy S, "Voltage sag /swell compensation using Z-source inverter based dynamic voltage restorer", *International conference on Emerging Trends in Electrical and Computer Technology, IEEE Xplore ICETECT*, 2011, pp. 268-273.

[11] Usha Rani P. and Rama Reddy S, "Dynamic Voltage restorer using Space Vector PWM Control Algorithm", European Journal of Scientific Research, Vol.56, No.4, 2011, pp.462-470

[12] Usha Rani P, "Modeling And Simulation Of Interline Dynamic Voltage Restorer Using SVPWM Technique", Journal of Theoretical and Applied Information Technology, Vol.60, No.1, 2014, pp.34-38

[13] Usha Rani P, "Multilevel Inverter Based Dynamic Voltage Restorer for Voltage Sag Compensation", Australian Journal of Basic and Applied Sciences, Vol.8, No.3, 2014, pp.146-150

[14] Usha Rani P and Smitha, "Digital Simulation of MLI based Dynamic Voltage Restorer for Voltage Sag Compensation", International Journal of Scientific & Engineering Research, Vol.5, No.6, 2014, pp.30-33.

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