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Implementation of High Speed Adder using DLATCH

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ABSTRACT

Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. The CSLA is used in many systems to overcome the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. But the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA). Due to the rapidly growing mobile industry not only the faster arithmetic unit but also less area and low power arithmetic units are needed. The modified CSLA architecture has developed using Binary to Excess-1 converter (BEC). This paper proposes an efficient method which replaces the BEC using D latch. Designs were developed using structural VHDL and synthesized in Xilinx 13.2 with reference to FPGA device XC3S500E.

Keywords: Field Programmable Gate Array (FPGA), D-Latch, Area Efficient, Carry Select Adder (CSLA), Square-Root CSLA (SQRT CSLA)

INTRODUCTION

Design of area efficient high speed data path logic systems are one of the most essential areas of research in VLSI. In digital adders, the speed of addition is controlled by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position was summed and a carry propagated into the next position. Bedriji proposed [1] that the problem of carry propagation delay is overcome by independently generating multiple radixes carries and using this carries to select between simultaneously generated sums. Akhilash Tyagi introduced a scheme to generate carry bits with block carry in 1 from the carries of a block with block carry in 0 [4]. Chang and Hsiao proposed [3] that instead of using dual Ripple Carry Adder a Carry Select Adder scheme using an add one circuit to replace one RCA. Youngioon Kim and Lee Sup Kim introduced a multiplexer based add one circuit was proposed to reduce the area with negligible speed penalty. Yajuan He et al proposed an area efficient Square-root CSLA (SQRT CSLA) scheme based on a new first zero detection logic [9]. Ramkumar et al proposed a Binary to Excess-1 Converter (BEC) method to reduce the maximum delay of carry propagation in final stage of carry save adder [2]. Ramkumar and Harish proposed [8] BEC technique, which is a simple and efficient gate level modification to significantly reduce the area of SQRT CSLA. Padma Devi et al proposed [10] modified CSLA designed in different stages which reduces the area. CSLA is used in many computational systems to relieve the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum [1].However, the CSLA is not area efficient because it uses multiple pairs of RCA to generate partial sum and carry by considering carry in 0 and carry in 1, then the final sum and carry are selected by the multiplexers (Mux).The basic idea of this work is to use BEC instead of RCA with carry in 1 in the regular CSLA to achieve lower area [2], [3] and [4]. The main benefit of BEC comes from the lesser number of logic gates than the n-bit Full Adder (FA). The details of BEC are discussed in section 3. Section 2 also deals with the area evaluation methodology of the basic adder blocks and presents the detailed structure and the function of the BEC. The CSLA has been chosen for

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comparison with the proposed design as it has a lower area [5], [6]. The area evaluation methodology of the regular Linear CSLA and modified Linear CSLA are presented in section IV. The area evaluation methodology of the regular SQRT CSLA and modified SQRT CSLA are presented in section 5. The FPGA implementation details and results are analysed in section 6. Finally this work is concluded in section 7.

AREA EVALUATION METHODOLOGY OF THE BASIC ADDER BLOCKS

An XOR gate is shown in Fig. 1, which is implemented by using AND, OR and Inverter (NOT). The gates between the dotted lines are performing the operations in parallel. The area evaluation methodology considers all gates to be made up of AND, OR and Inverter (AOI), each having are The area evaluation is done by counting the total gates required for each logic block. Based on the CSLA blocks of 2:1 Mux, Half Adder (HA) and Full Adder (FA) are evaluated and listed in Table I.

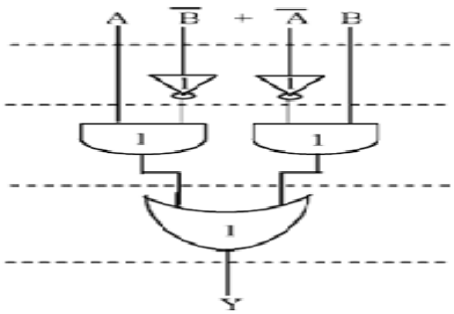

Fig1. *Area Evaluation of an XOR Gate*

Table1. *Area Count of the Basic Blocks of CSLA*

CSLA	AREA COUNT
XOR	5
2:1 MUX	4
HA	6
FA	13

BINARY TO EXCESS-1 CONVERTER (BEC)

The main idea of this work is to use BEC with carry in=1 in order to reduce the area of t CSLA as well as regular SQRT CSLA. To RCA, an n+1-bit BEC is required. A structure of 3-bit BEC are shown in Fig. 2 and Table II, Boolean expressions for 3-bit BEC is shown functional symbols ~ NOT, & AND, ^ XOR)

$$X0 = \sim B0 \quad (1)$$

$$X1 = B0 \wedge B1 \quad (2)$$

$$X2 = B2 \wedge (B0 \,\&\, B1) \quad (3)$$

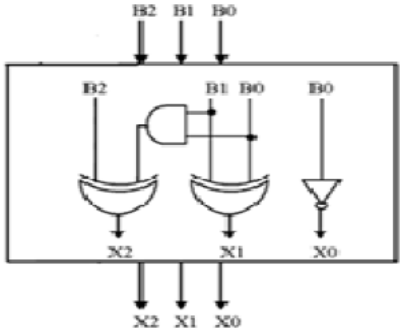

Fig2. *BEC Block*

Table2. *Function Table of The 3-bit BEC*

B[2:0]	X[2:0]
000	001
001	010
010	011
011	100
100	101
101	110
110	111
111	000

AREA EVALUATION METHODOLOGY OF REGULAR 16-BIT LINEAR AS WELL AS SQRT CSLA

The structure of the 16-bit regular Linear CSLA is shown in Fig. 3. It has 4 groups of same size CA. Each group contains dual RCA and Mux. It accomplishes the addition by adding small portions of bits (each of equal size) and wait for the carry to complete the calculation. Both sum and carry are calculated for both possible solutions. The Linear carry select adder is constructed by chaining a number of equal length adder stages. Here the equal size of inputs is given to each block of the adder. The steps leading to the evaluations are given here. In the regular Linear CSLA, the group2 has two sets of 4-bit RCA. The selection input of 10:5 Mux is c3.If the c3=0, the mux select first RCA output otherwise it select second RCA output.

The output of group2 is Sum [7:4] and carryout, c7.Then the area count of group2 is determined as follows

Gate count = 117 (FA+HA+MUX)

FA = 91 (7 * 13)

HA = 6 (1 * 6)

Mux = 20 (5 * 4)

Similarly the estimated area of the other groups in the regular Linear CSLA are evaluated and listed in Table3.

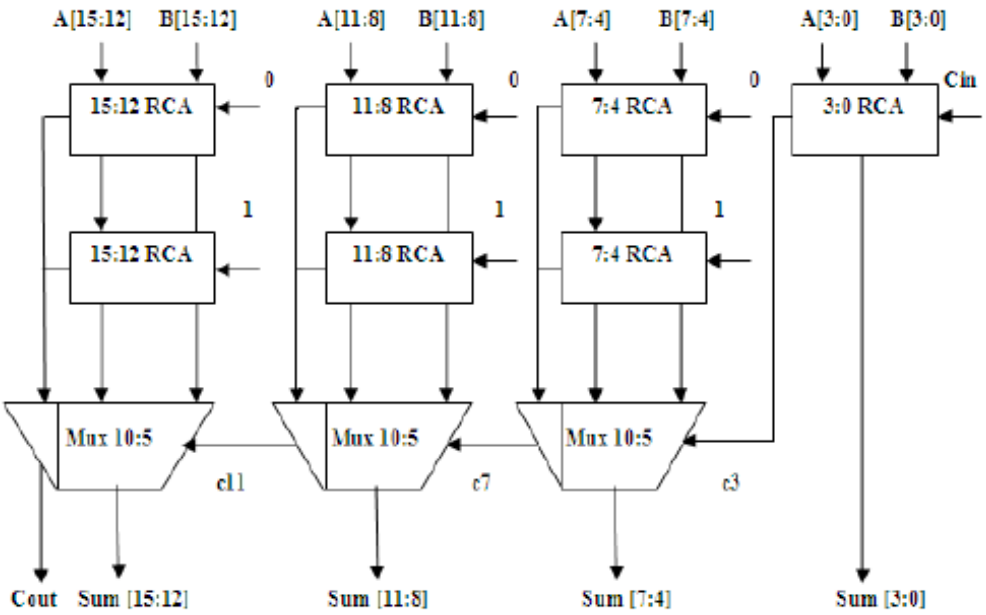

Fig3. *Regular 16-bit Linear CSLA*

Table3. *Area Count of The 16-bit Regular Linear CSLA Groups*

GROUP	AREA COUNT
GROUP1	52
GROUP2	117
GROUP3	117
GROUP4	117

The structure of the 16-bit regular SQRT CSLA is Shown in Fig. 4. It has 5 groups of different size RCA. Each group contains dual RCA and Mux. The linear carry select adder has two disadvantages there are high area usage and high time delay. These disadvantages of linear carry select adder can be rectified by SQRT CSLA. It is an improved one of linear CSLA. The time delay of the linear adder can decrease by having one more input into each set of adders than in the previous set. This is called a Square Root Carry Select Adder. Square Root carry select adder is constructed by equalizing the delay through two carry chains and the block-multiplexer signal from previous stage. The steps leading to the evaluations are given here. In the regular SQRT CSLA, the group2 has two sets of 2-bit RCA. The selection input of 3:2 Mux is c1. If the c1 = 0, the Mux select first RCA output otherwise it select second RCA output. The output of group2 are Sum [3:2] and carryout, c3. Then the area count of group2 is determined as follows:

Gate count = 57 (FA + HA + Mux)

FA = 39 (3 * 13)

HA = 6 (1 * 6)

Mux = 12 (3 * 4)

Similarly the estimated area of the other groups in the regular SQRT CSLA are evaluated and listed in Table 4.

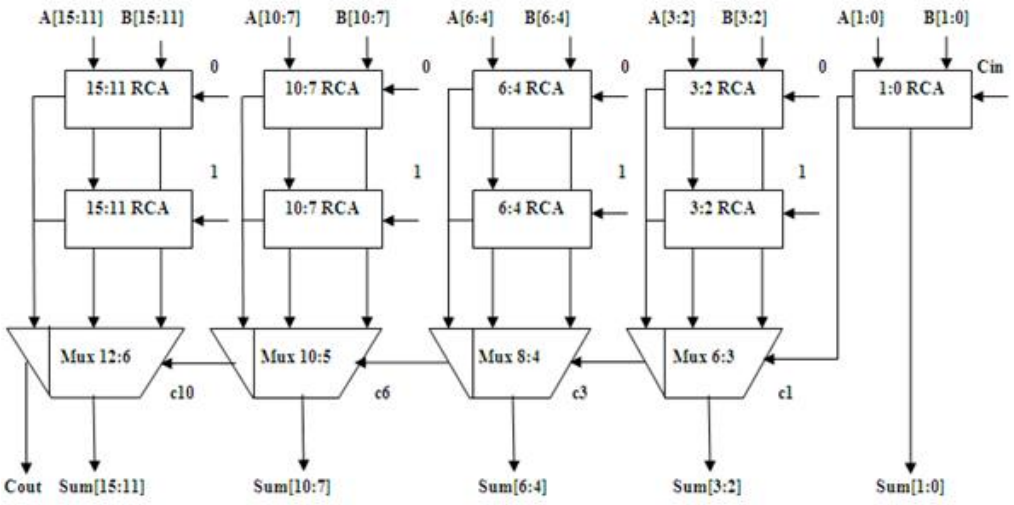

Fig4. *Regular 16-bit SQRT CSLA*

Table4. *Area Count of The 16-bit Regular SQRT CSLA Groups*

GROUP	AREA COUNT
GROUP1	26
GROUP2	57
GROUP3	87
GROUP4	117
GROUP5	147

AREA EVALUATION METHODOLOGY OF MODIFIED 16-BIT LINEAR AS WELL AS SQRT CSLA

The structure of the proposed 16-bit Linear and SQRT CSLA using BEC for RCA with carry in = 1 to optimize the area is shown in Fig. 5 and Fig. 6 respectively. The 16-bit modified Linear CSLA has 4 groups of same size RCA and BEC. Each group contains one RCA, one BEC and Mux. In the modified Linear CSLA, the group2 has one 4-bit RCA which has 3 FA and 1 HA for carry in = 0. Instead of another 4-bit RCA with carry in = 1 a 5-bit BEC is used which adds one to the output from 4-bit RCA. The selection input of 10:5 Mux is c3. If the c3 = 0, the Mux select RCA output otherwise it select BEC output. The output of group2 are Sum [7:4] and carryout, c7. Then the area count of group2 is determined as follows:

Gate count = 89 (FA + HA + Mux + BEC)

FA = 39 (3 * 13)

HA = 6 (1 * 6)

Mux = 20 (5 * 4)

NOT = 1

AND = 3 (3 * 1)

XOR = 20 (4 * 5)

BEC (5-BIT) = NOT + AND + XOR = 24

Similarly the estimated area of the other groups in the modified Linear CSLA are evaluated and listed in Table 5.

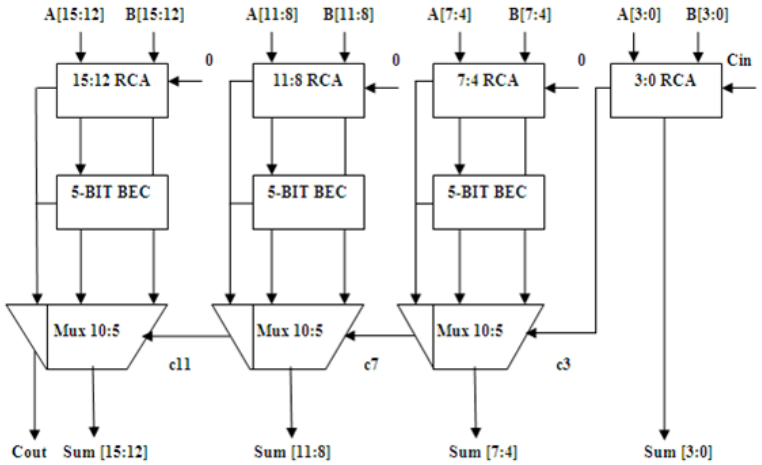

Fig5. *Modified 16-bit Regular CSLA*

Table5. *Area Count of The 16-bit Modified Linear CSLA Groups*

GROUP	AREA COUNT
Group1	52
Group2	89
Group3	89
Group4	89

The structure of the 16-bit modified SQRT CSLA is shown in Figure. 6. It has 5 groups of different size RCA and BEC. Each group contains one RCA, one BEC and MUX. In the modified SQRT CSLA, the group2 has one 2-bit RCA which has 1 FA and 1 HA for carry in = 0. Instead of another 2-bit RCA with carry in = 1 a 3-bit BEC is used which adds one to the output from 2-bit RCA. The selection input of 6:3 Mux is c3. If the c3 = 0, the Mux select RCA output otherwise it select

BEC output. The output of group2 are Sum [3:2] and carryout,c3. Then the area count of group2 is determined as follows:

Gate count = 43 (FA + HA + Mux + BEC)

FA = 13 (1 * 13)

HA = 6 (1 * 6)

Mux = 12 (3 * 4)

NOT = 1

AND = 1

XOR = 10 (2 * 5)

BEC (3-BIT) = NOT + AND + XOR = 12

Similarly the estimated area of the other groups in the modified SQRT CSLA are evaluated and listed in Table 6.

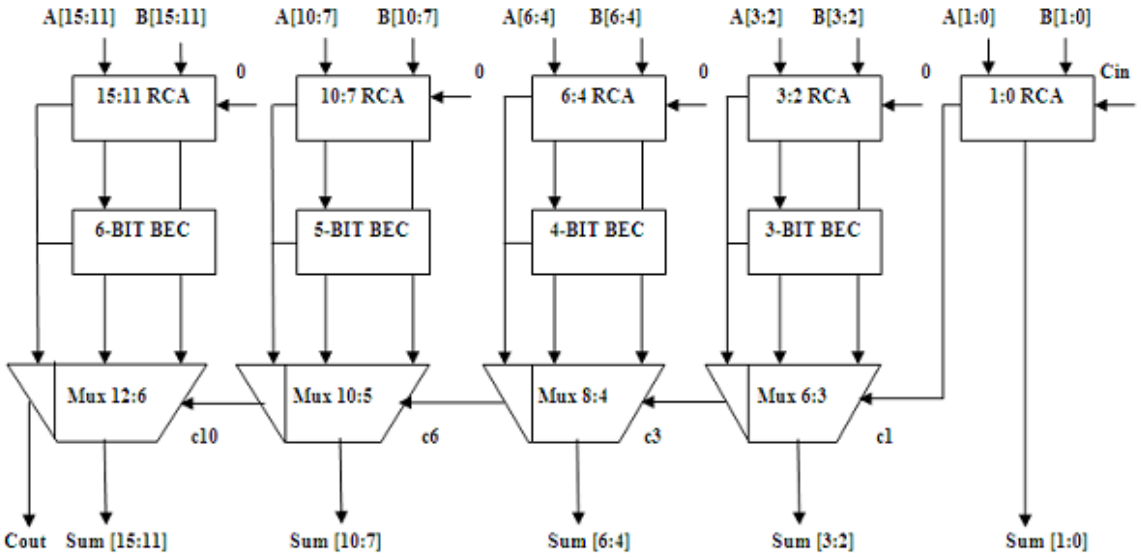

Fig6. *Modified 16-bit SQRT CSLA*

Table6. *Area Count of The 16-bit Modified SQRT CSLA Groups*

GROUP	AREA COUNT
Group1	26
Group2	43
Group3	66
Group4	89
Group5	113

Comparing Tables 3 and 4 with Tables 5 and 6, it is clear that the proposed modified Linear as well as SQRT CSLA save 84 gate and 97 gate areas than the regular Linear CSLA and regular SQRT CSLA respectively.

MODIFIED 16-BIT CSLA USING D-LATCH

This method replaces the BEC add one circuit by D-latch with enable signal. Latches are used to store one bit information. Their outputs are constantly affected by their inputs as long as the enable signal is asserted. In other words, when they are enabled, their content changes immediately according to their inputs. D-latch and it's waveforms are shown in Fig.7&8.

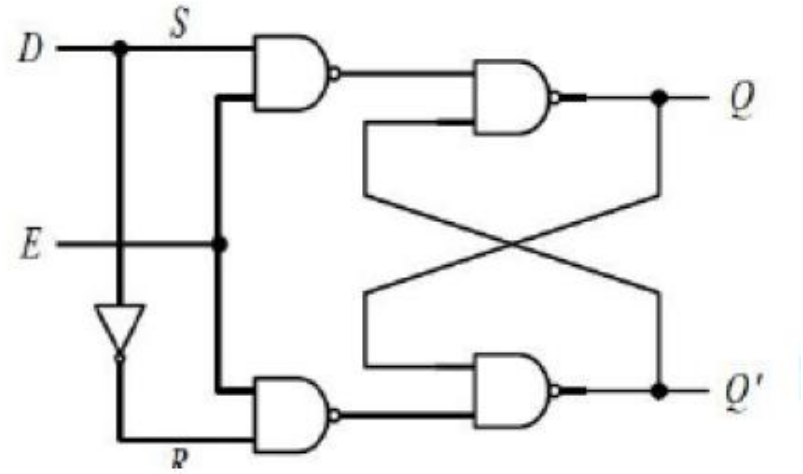

Fig7. *D Latch*

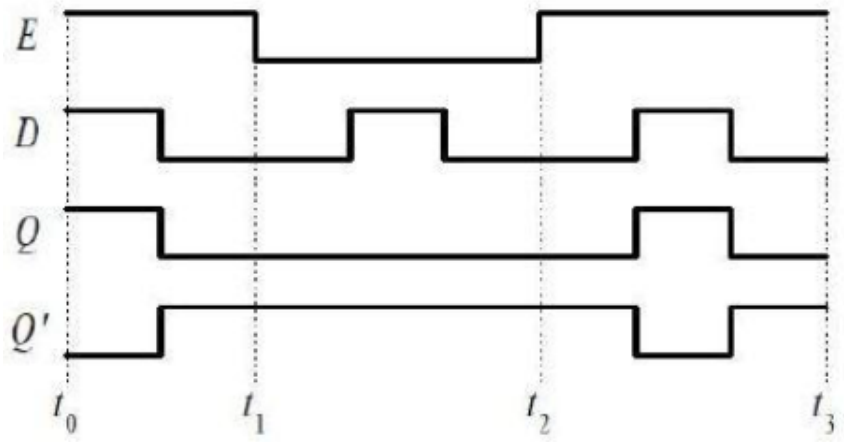

Fig8. *Input and Output Waveforms*

The architecture of proposed 16-b CSLA is shown in Figure 9. It has different five groups of different bit size RCA and D-Latch. Instead of using two separate adders in the regular CSLA, in this method only one adder is used. Each of the two additions is performed in one clock cycle. This is 16-bit adder in which least significant bit (LSB) adder is ripple carry adder, which is 2 bit wide. The upper half of the adder i.e., most significant part is 14-bit wide which works according to the clock. Whenever clock goes high addition for carry input one is performed. When clock goes low then carry input is assumed as zero and sum is stored in adder itself. From the Fig.9 it can understand that latch is used to store the sum and carry for Cin=1 and cin=0.Carry out from the previous stage i.e., least significant bit adder is used as control signal for multiplexer to select final output carry and sum of the 16-bit adder. If the actual carry input is one, then computed sum and carry latch is accessed and for carry input zero MSB adder is accessed. Cout is the output carry.

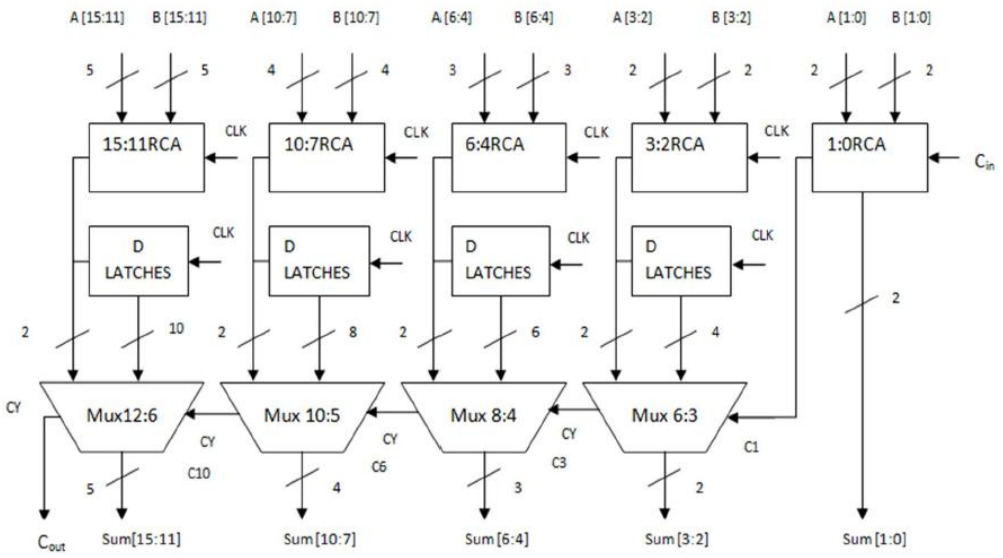

Fig9. *Modified CSLA Using D Latch*

The group 2 performed the two bit addition which is a2 with b2 and a3 with b3. This is done by two full adder (FA) named FA2 and FA3 respectively. The third input to the full adder FA2 is the clock instead of the carry and the third input to the full adder FA3 is the carry output from FA2. The group 2 structure has five D-Latches in which four are used for store the sum2 and sum3 from FA2 and FA3 respectively and the last one is used to store carry. Multiplexer is used for selecting the actual sum and carry according to the carry is coming from the previous stage. The 6:3 multiplexer is the combination of 2:1 multiplexer. When the clock is low a2 and b2 are added with carry is equal to zero. Because of low clock, the first D-Latch is not enabled. The second D-Latch store the sum wit cin =0 by using inverted clock enable. When the clock is high, the addition is performed with carry is equal to one. The other D-Latches enabled and store the sum and carry for carry is equal to one. According to the value of c1 whether it is 0 or 1, the multiplexer selected the actual sum and carry.

FPGA IMPLEMENTATION RESULTS

This work has been developed using VHDL. It was simulated and synthesized using Xilinx 13.2. This design was implemented Spartan 3E kit. Fig. 10(a), 10(b), 10(c), 10(d), 10(e) show the simulation results of regular 16-bit Linear CSLA, regular 16-bit SQRT CSLA, modified 16-bit Linear CSLA, modified 16-bit SQRT CSLA and 16-bit Modified CSLA using D-latch respectively.

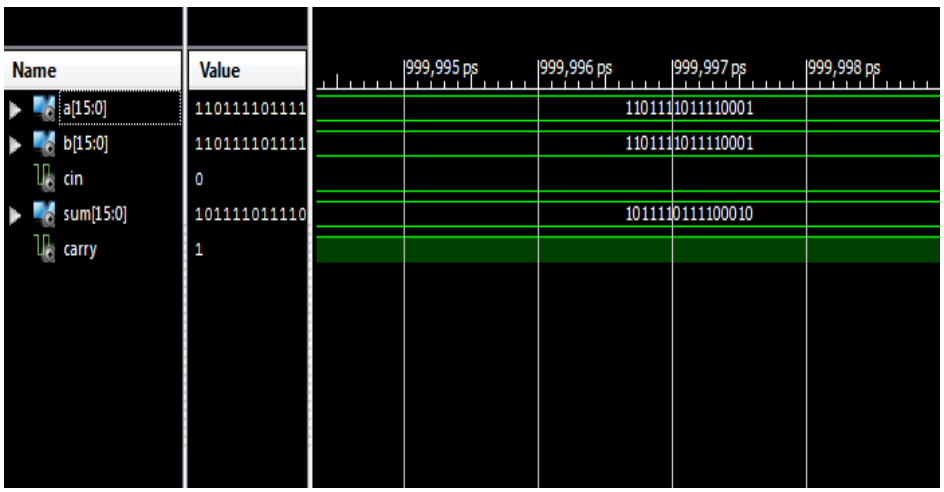

Fig10(a). *16-bit Regular Linear CSLA*

It is clear that the area of the 16-bit proposed modified SQRT CSLA is reduced when compared with the area of other CSLAs. The Modified CSLA with D-Latches is going to increase the speed compare to all previous works.

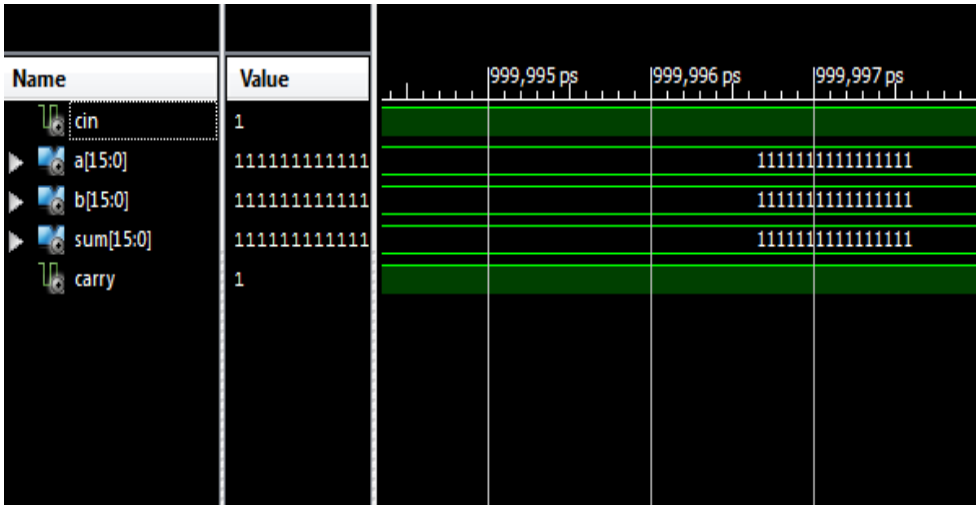

Fig10 (b). *16-bit Regular SQRT CSLA*

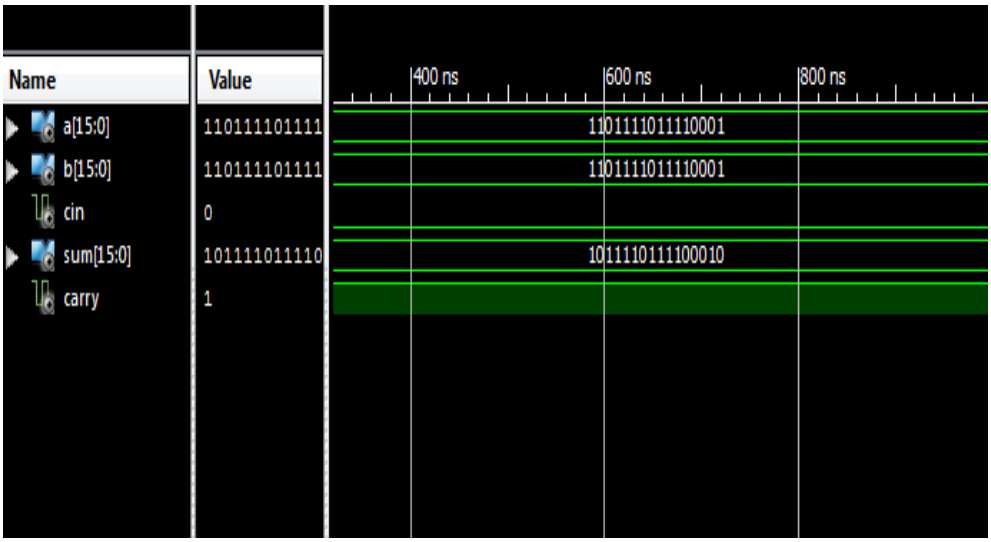

Fig10(c). *16-bit Modified Linear CSLA*

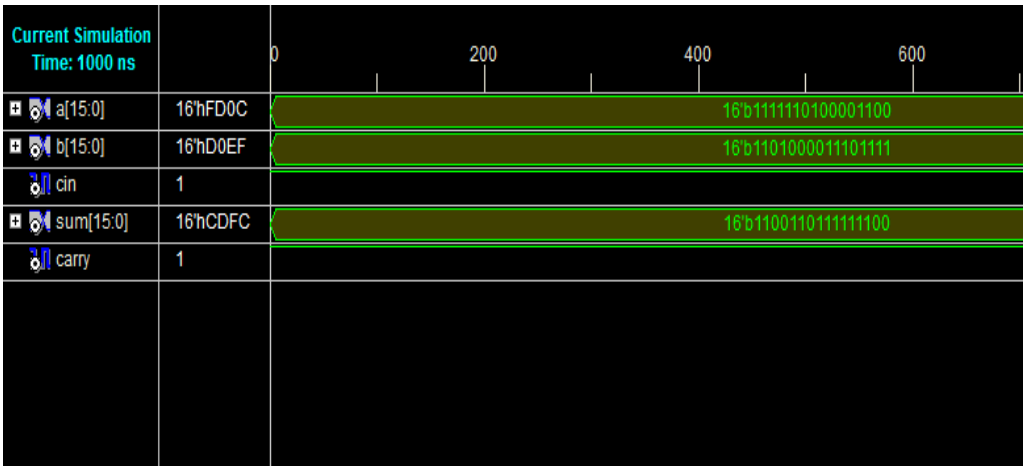

Fig 10(d). *16-bit Modified Sqrt CSLA*

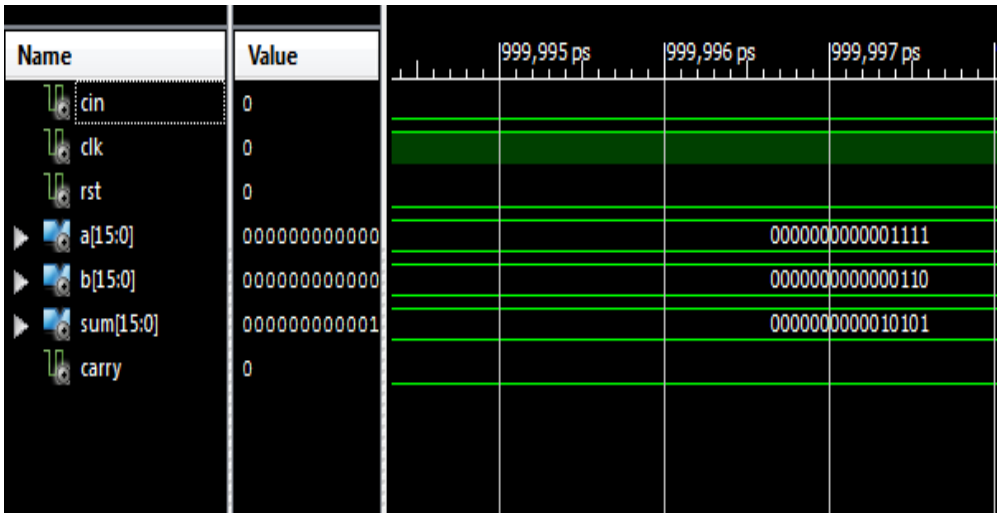

Fig10(e). *16-bit Modified CSLA using D-Latch*

CONCLUSION

This project presented a simple approach to reduce the delay of CSLA architecture. The previous work Modified CSLA is used to reduce the area. The reduced number of gates of this work offers the great advantage in the reduction of area. The area (gate count) of the Modified SQRT CSLA is significantly reduced when compared with Regular Linear. The delay is slightly increased than the previous one. Our proposed project Modified CSLA with D-Latches is increases the speed compare to all previous works. Hence Modified CSLA with D-Latch considered as a high speed adder.

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