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Effective Area Comparative Analysis of Efficient Architecture for Carry Select Adder (CSLA)

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ABSTRACT

Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. The CSLA is used in many systems to overcome the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. But the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA). Due to the rapidly growing mobile industry not only the faster arithmetic unit but also less area and low power arithmetic units are needed. The modified CSLA architecture has developed using Binary to Excess-1 converter (BEC). This paper proposes 128bit modified CSLA. Designs were developed using structural VHDL and synthesized in Xilinx 13.2 with reference to FPGA device XC3S500E.

Keywords: Field Programmable Gate Array (FPGA), Area efficient, Carry Select Adder (CSLA), Square-root CSLA (SQRT CSLA).

INTRODUCTION

Design of area efficient high speed data path logic systems are one of the most essential areas of research in VLSI. In digital adders, the speed of addition is controlled by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position was summed and a carry propagated into the next position. Bedriji proposed [1] that the problem of carry propagation delay is overcome by independently generating multiple radixes carries and using this carries to select between simultaneously generated sums. Akhilash Tyagi introduced a scheme to generate carry bits with block carry in 1 from the carries of a block with block carry in 0 [4]. Chang and Hsiao proposed [3] that instead of using dual Ripple Carry Adder a Carry Select Adder scheme using an add one circuit to replace one RCA. Youngioon Kim and Lee Sup Kim introduced a multiplexer based add one circuit was proposed to reduce the area with negligible speed penalty. Yajuan He et al proposed an area efficient Square-root CSLA (SQRT CSLA) scheme based on a new first zero detection logic [9]. Ram Kumar et al proposed a Binary to Excess-1 Converter (BEC) method to reduce the maximum delay of carry propagation in final stage of carry save adder [2]. Ram Kumar and Harish proposed [8] BEC technique, which is a simple and efficient gate level modification to significantly reduce the area of SQRT CSLA. Padma Devi et al proposed [10] modified CSLA designed in different stages which reduces the area. CSLA is used in many computational systems to relieve the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum [1].However, the CSLA is not area efficient because it uses multiple pairs of RCA to generate partial sum and carry by considering carry in 0 and carry in 1, then the final sum and carry are

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selected by the multiplexers (MUX).The basic idea of this work is to use BEC instead of RCA with carry in 1 in the regular CSLA to achieve lower area [2], [3] and [4]. The main benefit of BEC comes from the lesser number of logic gates than the n-bit Full Adder (FA). The details of BEC are discussed in section 3. Section 2 also deals with the area evaluation methodology of the basic adder blocks and presents the detailed structure and the function of the BEC. The CSLA has been chosen for comparison with the proposed design as it has a lower area [5], [6]. The area evaluation methodology of the regular Linear CSLA and modified Linear CSLA are presented in section IV. The area evaluation methodology of the regular SQRT CSLA and modified SQRT CSLA are presented in section 5. The FPGA implementation details and results are analysed in section 6. Finally this work is concluded in section 7.

Area Evaluation Methodology of the Basic Adder Blocks

An XOR gate is shown in Fig. 1, which is implemented by using AND, OR and Inverter (NOT). The gates between the dotted lines are performing the operations in parallel. The area evaluation methodology considers all gates to be made up of AND, OR and Inverter (AOI), each having are the area evaluation is done by counting the total gates required for each logic block. Based on the CSLA blocks of 2:1 Mux, Half Adder (HA) and Full Adder (FA) are evaluated and listed in Table I.

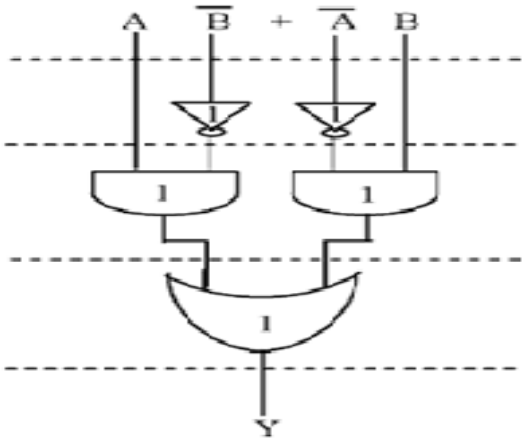

Fig1.*Area Evaluation of an XOR Gate*

Table1. *Area Count of The Basic Blocks of CSLA*

CSLA	AREA COUNT
XOR	5
2:1 MUX	4
HA	6
FA	13

BINARY TO EXCESS-1 CONVERTER (BEC)

The main idea of this work is to use BEC with carry in=1 in order to reduce the area of t CSLA as well as regular SQRT CSLA. To RCA, an n+1-bit BEC is required. A structure of 3-bit BEC are shown in Fig. 2 and Table II, Boolean expressions for 3-bit BEC is shown functional symbols ~ NOT, & AND, ^ XOR)

X0 = ~ B0 (1)

X1 = B0 ^ B1 (2)

X2 = B2 ^ (B0 & B1) (3)

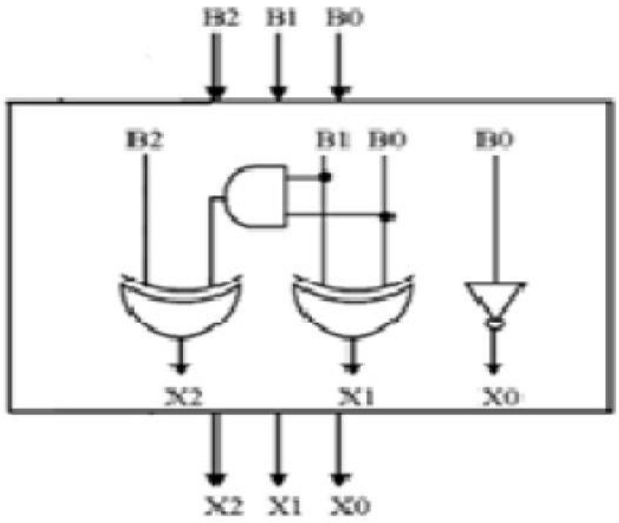

Fig2. *BEC Block*

Table2. *Function Table of The 3-bit BEC*

B[2:0]	X[2:0]
000	001
001	010
010	011
011	100
100	101
101	110
110	111
111	000

REGULAR 16-BIT SQRT CSLA

The structure of the 16-bit regular SQRT CSLA is shown in Fig. 4. It has 5 groups of different size RCA. Each group contains dual RCA and Mux. The linear carry select adder has two disadvantages there are high area usage and high time delay. These disadvantages of linear carry select adder can be rectified by SQRT CSLA. It is an improved one of linear CSLA. The time delay of the linear adder can decrease by having one more input into each set of adders than in the previous set. This is called a Square Root Carry Select Adder. Square Root carry select adder is constructed by equalizing the delay through two carry chains and the block-multiplexer signal from previous stage. The steps leading to the evaluations are given here. In the regular SQRT CSLA, the group2 has two sets of 2-bit RCA. The selection input of 3:2 Mux is c1. If the c1 = 0, the Mux select first RCA output otherwise it select second RCA output. The output of group2 are Sum [3:2] and carryout, c3. Then the area count of group2 is determined as follows:

Gate count = 57 (FA + HA + Mux)

FA = 39 (3 * 13)

HA = 6 (1 * 6)

Mux = 12 (3 * 4)

Similarly the estimated area of the other groups in the regular SQRT CSLA are evaluated and listed in Table 4.

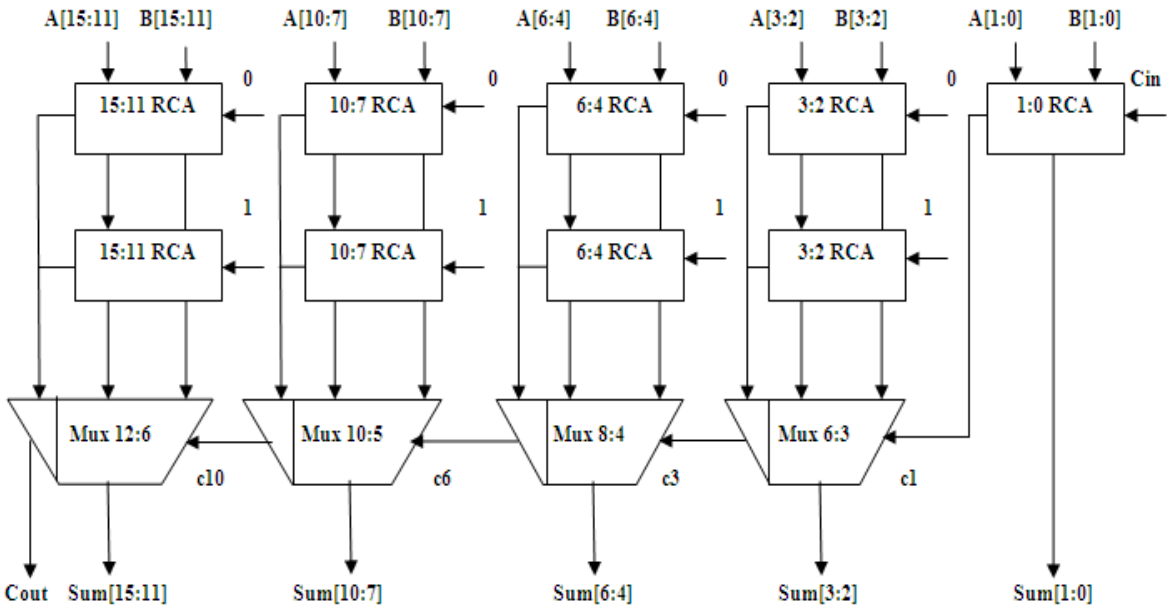

Fig4. *Regular 16-bit SQRT CSLA*

Table4. *Area Count of The 16-bit Regular SQRT CSLA Groups*

GROUP	AREA COUNT
GROUP1	26
GROUP2	57
GROUP3	87
GROUP4	117
GROUP5	147

MODIFIED 16-BIT SQRT CSLAT

The structure of the 16-bit modified SQRT CSLA is shown in Figure. 5. It has 5 groups of different size RCA and BEC. Each group contains one RCA, one BEC and MUX. In the modified SQRT CSLA, the group2 has one 2-bit RCA which has 1 FA and 1 HA for carry in = 0. Instead of another 2-bit RCA with carry in = 1 a 3-bit BEC is used which adds one to the output from 2-bit RCA. The selection input of 6:3 Mux is c3. If the c3 = 0, the Mux select RCA output otherwise it select

BEC output. The output of group2 are Sum [3:2] and carryout, c3. Then the area count of group2 is determined as follows:

Gate count = 43 (FA + HA + Mux + BEC)

FA = 13 (1 * 13)

HA = 6 (1 * 6)

Mux = 12 (3 * 4)

NOT = 1

AND = 1

XOR = 10 (2 * 5)

BEC (3-BIT) = NOT + AND + XOR = 12

Similarly the estimated area of the other groups in the modified SQRT CSLA are evaluated and listed in Table 6.

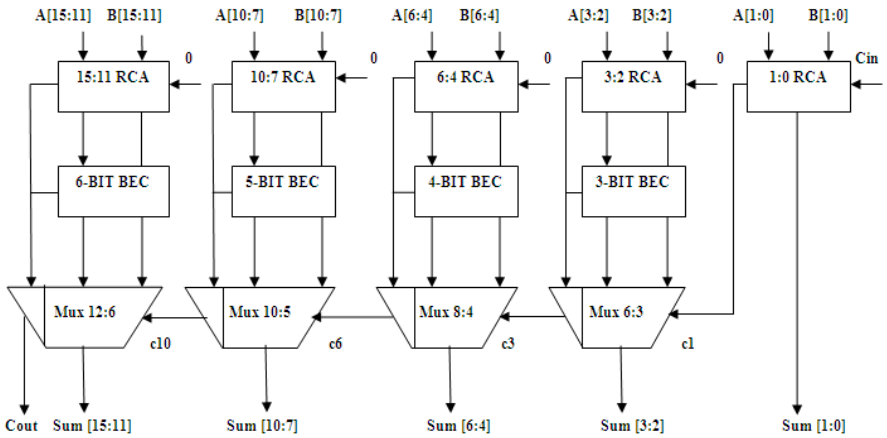

Fig5. *Modified 16-bit SQRT CSLA*

Table6. *Area Count of The 16-bit Modified SQRT CSLA Groups*

GROUP	AREA COUNT
Group1	26
Group2	43
Group3	66
Group4	89
Group5	113

MODIFIED 128-BIT CSLA

This architecture is similar to regular 64-bit SQRT CSLA, the only change is that, we replace RCA with Cin=1 among the two available RCAs in a group with a BEC. This BEC has a feature that it can perform the similar operation as that of the replaced RCA with Cin=1. Fig 7 shows the Modified block diagram of 64-bit SQRT CSLA. The number of bits required for BEC logic is 1 bit more than the RCA bits. The modified block diagram is also divided into various groups of variable sizes of bits with each group having the ripple carry adders, BEC and corresponding mux. As shown in the Fig.4, Group 0 contain one RCA only which is having input of lower significant bit and carry in bit and produces result of sum [1:0] and carry out which is acting as mux selection line for the next group, similarly the procedure continues for higher groups but they includes BEC logic instead of RCA with Cin=1.Based on the consideration of delay values, the arrival.

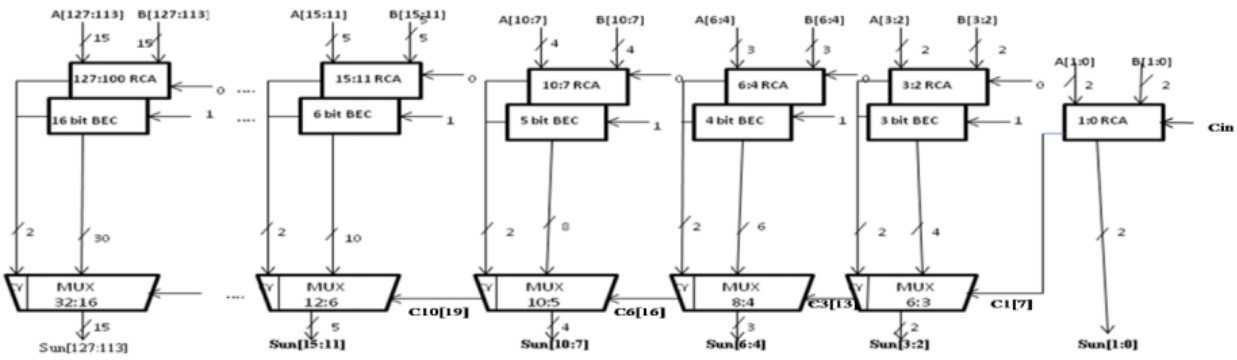

Fig7. *Modified 128bit SQRT CSLA*

SIMULATION RESULTS

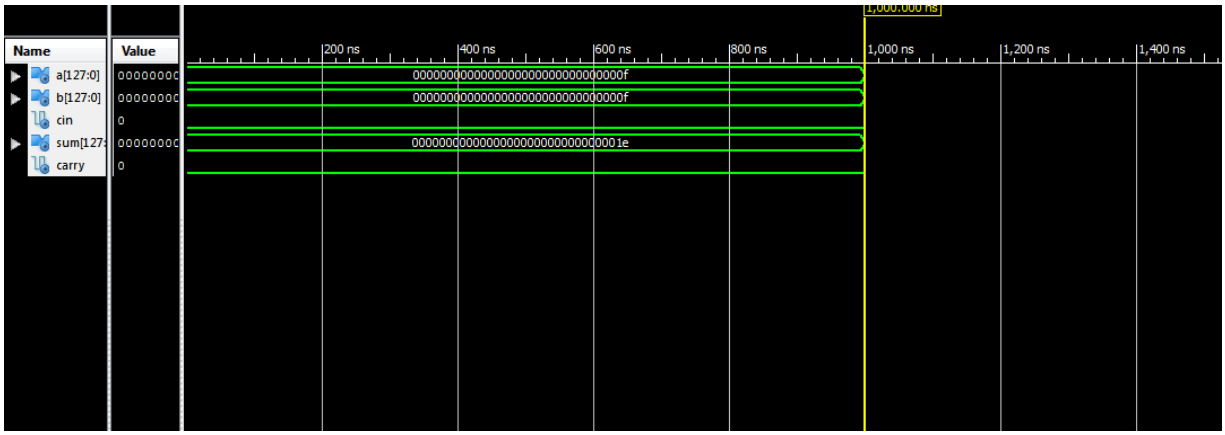

Fig8. *128-bit Modified Sqrt CSLA*

CONCLUSION

The Modified CSLA is used to reduce the area. The reduced number of gates of this work offers the great advantage in the reduction of area. The area (gate count) of the Modified SQRT CSLA is significantly reduced when compared with Regular.

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